

By default, if the Core Type cell is left empty, the spreadsheet will select the EE16 core. The user can change this selection and choose an alternate core from a list of commonly available cores suitable for the output power (shown in Table 4). The values shown are based on an assumed output voltage of 6 V, 4 primary winding layers and the default input parameters as described in Step 1. Changes to these values will change the power capability of a given core size, therefore Table 4 should be used for guidance only.

Core Size	Commonly Used	Suggested Power Range	
		100/115 or 85-265 VAC	230 VAC Only
EE8	No	< 1 W	< 1 W
EP10	No	< 1.75 W	< 1.75 W
EE10	No	< 2 W	< 2 W
EF12.6	Yes	< 3.3 W	< 3.3 W
EE13	Yes	< 4 W	< 4 W
EE16	Yes	< 5 W	< 6 W
EE1616	Yes	< 5.5 W	< 7 W
EE19	Yes	< 5.6 W	< 7.1 W
EF20	Yes	< 6 W	< 8 W
EF25	Yes	< 6 W	< 9 W

Table 4. Maximum Power Capability of Cores Used in Flyback Topology

be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical however, the total margin divided by 2 should still be entered.

As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin, more than 4 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire for the secondary winding.

Primary Layers, L

By default, if the override cell is empty, a value of 2 is assumed. Primary layers should be in the range of $1 < L < 4$, and in general it should be the lowest number that meets the primary current density limit (CMA) of 150 Cmil/Amp. Values above 4 layers are possible, but the increased leakage inductance and physical fit of the windings should be considered.

For *Clampless* designs without a bias winding, 2 primary layers must be used. This is to ensure sufficient primary capacitance to limit the peak Drain voltage below the BV_{DSS} rating of the internal MOSFET.

Secondary Turns, N_s

By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density, B_M , is kept below the recommended maximum. In general, it is not necessary to enter a number in

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type		EE16		Suggested smallest commonly available core
Core		EE16	P/N:	PC40EE16-Z
Bobbin		EE16_BOBBIN	P/N:	EE16_BOBBIN
AE		0.192	cm ²	Core Effective Cross Sectional Area
LE		3.5	cm	Core Effective Path Length
AL		1140	nH/T ²	Ungapped Core Effective Inductance
BW		8.6	mm	Bobbin Physical Winding Width
M		0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		2		L > 2 or L < 1 not recommended for Clampless designs with no Bias windings. Enter L = 2
NS		11		Number of Secondary Turns
NB		N/A		Bias winding not used
VB		N/A	Volts	Bias winding not used
PIVB		N/A	Volts	N/A - Bias Winding not in use

Figure 5. Transformer Core and Construction Variables Section of Spreadsheet.

The gray override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet.

Safety Margin, M (mm)

For designs that require isolation but are not using triple insulated wire for the secondary winding, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required; therefore a value of 3.1 mm would

the override cell except in designs where a higher operating flux density is acceptable (see Minimizing Audible Noise section for an explanation of B_M limits).

Calculated Bias Winding Turns and Voltage N_B, V_B

Where a bias winding is used, the number of turns and voltage developed are displayed. The relatively large default number of turns allows the bias to be used as a shield winding for reduced EMI. If desired, the number of turns can be adjusted by entering a value into the gray override cell.

The variables described in step 3 are found in the “Enter Transformer Core/Construction Variables” section of the spreadsheet (see Figure 5).

Step 4 – Iterate Transformer Design and Generate Transformer Design Output

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or send to a vendor for samples.

The key transformer electrical parameters are:

Primary Inductance, L_p (μH)

This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{P_TOLERANCE}$ (%)

This is the assumed primary inductance tolerance. A value of $\pm 10\%$ is used by default, however if specific information is known from the transformer vendor, then this may be overridden by entering a new value in the gray override cell.

Maximum operating flux density, B_M (Gauss)

The cycle skipping mode of operation used in *LinkSwitch-XT* can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 1500 Gauss (150 mT). Following this guideline, and using the standard transformer production technique of dip varnishing, practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Audible noise may also be created by ceramic capacitors that use dielectrics such as

Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric, for example a film type. Flux densities above 3000 Gauss (300 mT) are not recommended.

Other transformer parameters calculated in the spreadsheet are:

N_p - Primary Winding Number of Turns

A_{LG} (nH/T^2) - Gapped Core Effective Inductance

B_{AC} (Gauss) - AC Flux Density for Core Loss Curves (0.5 x Peak to Peak)

μ_r - Relative Permeability of Ungapped Core

L_G (mm) - Gap Length ($L_G > 0.1$ mm).

B_{WE} (mm) - Effective Bobbin Width (Accounts for Margin tape if used)

O_D (mm) - Maximum Primary Wire Diameter including insulation

INS (mm) - Estimated Total Insulation Thickness (= 2 * film thickness)

DIA (mm) - Bare conductor diameter

AWG - Primary Wire Gauge (Rounded to next smaller standard AWG value)

CM (Cmils) - Bare conductor effective area in circular mils

CMA (Cmils/Amp) - Primary Winding Current Capacity (150 < CMA < 500)

Variables described in step 4 can be found under the “Transformer Primary Design Parameters” section of the spreadsheet (see Figure 6).

Step 5 – Selection of Input Stage

The input stage comprises a fusible element(s), input rectification and line filter network. The fusible element can be either a fusible resistor, fuse or make use of Power Integration’s *Filterfuse* technique. Here, the input inductor may also used as a fuse, typically requiring the addition of a heatsink shroud to prevent incandescent material being ejected during a fault. By using *Filterfuse*, the input stage can be simplified in saving the cost of a fusible resistor, but requiring a larger single input capacitor. However, please verify with a safety engineer or

TRANSFORMER PRIMARY DESIGN PARAMETERS			
LP		2563	$\mu\text{Henries}$ Typical Primary Inductance. +/- 10%
LP_TOLERANCE		10	% Primary inductance tolerance
NP		135	Primary Winding Number of Turns
ALG		140	nH/T^2 Gapped Core Effective Inductance
BM		1479	Gauss Maximum Operating Flux Density, $B_M < 1500$ is recommended
BAC		624	Gauss AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
μ_r		1654	Relative Permeability of Ungapped Core
LG		0.15	mm Gap Length ($L_G > 0.1$ mm)
BWE		17.2	mm Effective Bobbin Width
OD		0.13	mm Maximum Primary Wire Diameter including insulation
INS		0.03	mm Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.10	mm Bare conductor diameter
AWG		39	AWG Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		13	Cmils Bare conductor effective area in circular mils
CMA		242	Cmils/Amp Primary Winding Current Capacity (150 < CMA < 500)

Figure 6. Transformer Primary Design Parameters Section of Design Spreadsheet.

P_{OUT}	$\leq 1\text{ W}$	$\leq 3\text{ W}$		
Suggested 85-265 VAC Input Stage				
Component Selection Guide	R_{F1} : 8.2 Ω , 1 W Fusible R_{F2} : 100 Ω , 0.5 W, Flameproof C_{IN1} , C_{IN2} : $\geq 3.3\ \mu\text{F}$, 400 V each D_{IN1} , D_{IN2} : 1N4007, 1 A, 1000 V	R_{F1} : 8.2 W, 1 W Fusible L_{IN} : 470 μH -2.2 mH, (0.05 A-0.3 A) C_{IN1} , C_{IN2} : $\geq 4\ \mu\text{F}/W_{OUT}^{\dagger}$, 400 V each D_{IN1} , D_{IN2} : 1N4007, 1 A, 1000 V	$L1, L2^*$: 3.3 μH , 0.06 A Filterfuse [®] $C1$: $\geq 5\ \mu\text{F}/W_{OUT}^{\dagger}$, 400 V D_{IN1} : 1N4937, 600 V D_{IN2} : 1N4007, 1000 V	R_{F1} : 8.2 W, 1 W Fusible L_{IN} : 470 μH -2.2 mH, (0.05 A-0.3 A) C_{IN1} , C_{IN2} : $\geq 2\ \mu\text{F}/W_{OUT}^{\dagger}$, 400 V each D_{IN1} - D_{IN4} : 1N4007, 1 A, 1000 V
Comments	**Increase value to meet required differential line	**Increase value to meet required differential line	*Check for safety agencies approval **Increase value to meet required differential line surge performance †Second inductor may be required in <i>Clampless</i> designs	**Increase value to meet required differential line surge

Table 5. Input Filter Recommendation Based on Total Output Power.

agency if *Filterfuse* is acceptable. *Clampless* designs $\geq 2\text{ W}$ without a bias winding may require an additional inductor for acceptable conducted EMI.

If a fusible resistor is selected, it should be a flameproof type and, depending on the differential line input surge requirements, a wire-wound type may be required. Care should be taken in using metal or carbon film types as these can fail simply due to the inrush current when AC is connected to the supply.

Designs using a Y-capacitor require the EMI filter impedance to be placed on the appropriate side of the input. Therefore when Y capacitor is returned to the DC rail, the fusible resistor(s) *Filterfuse* should be placed in the opposite side of the input.

For designs $< 1\text{ W}$, it is generally lower cost to use half-wave rectification; and $\geq 1\text{ W}$, full-wave rectification. However if *Filterfuse* is used, even above 1 W, half wave rectification may lower cost and should be selected accordingly.

	<i>Clampless</i>		External Clamp
	$\leq 2\text{ W}$	$2\text{ W} < P_o \leq 2.5\text{ W}$	
Bias winding required	N	Y	N
Device	LNK362 only		Any
Primary layers	= 2 (no bias winding) ≤ 4 (with bias winding)	≤ 4	≤ 4
V_{OR} (V)	≤ 90	≤ 130	≤ 130
Recommended Transformer Parameters	Leakage inductance $< 90\ \mu\text{H}$ Primary capacitance $\geq 50\ \text{pF}$	No restriction	
Leakage ring effect on EMI	High	Medium	Low

Table 6. Factors to be Considered While Deciding Between a *Clampless* or External Clamp Design.

Type	RCD	Zener
Suggested Primary Clamp		
Advantages	<ul style="list-style-type: none"> • Lower cost • Lower EMI 	<ul style="list-style-type: none"> • Lower parts count • Lower no-load consumption
Component Selection Guide	<ul style="list-style-type: none"> • D_{CLAMP} (1 A, 600 V) <ul style="list-style-type: none"> - UF4005, 1N3947 or 1N4007GP - 1N4007 improves EMI and efficiency but must be glass passivate type (1N4007GP) • R_{CLAMP2} <ul style="list-style-type: none"> - Not necessary when using ultra-fast (UF4005) or fast diode (1N4937) - A value in the range of 50 Ω to 330 Ω, 1/4 W should be used with a slow diode (1N4007GP) to limit reverse pull out current 	
	<ul style="list-style-type: none"> • R_{CLAMP} <ul style="list-style-type: none"> - 47 kΩ to 200 kΩ, 1/4 W or 1/2 W • C_{CLAMP} <ul style="list-style-type: none"> - 390 pF to 2.2 nF, ≥ 400 V ceramic or film (Note ceramic capacitors may create audible noise) 	<ul style="list-style-type: none"> • VR_{CLAMP} <ul style="list-style-type: none"> - Select voltage to be $1.5 \bullet V_{OR}$ with a power rating of 0.5 W to 1 W (P6KExxx and BZY97Cxxx series are good examples of suitable Zener diodes)

Table 7. Primary Clamp Recommendation (for Output Power > 2.5 W).

The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles the differential surge-withstand as the surge voltage is shared across two diodes. In designs using a single input capacitor at least one of the input diodes should be a fast type ($t_{rr} \leq 200$ ns). This reduces ringing and associated increase in EMI. Table 5 shows the recommended input stage based on output power for a universal input design while Table 2 shows how to adjust the input capacitance for other input voltage ranges.

Step 6 – Selection of **LinkSwitch-XT** External Components

LinkSwitch-XT requires a 0.1 μ F / 50 V capacitor across the BYPASS and SOURCE pins.

Step 7 – Selection of Primary Clamp Circuit

For output powers of 2.5 W or below and using the LNK362, it

is possible to eliminate external clamp components by careful design of the transformer and bias winding. For *Clampless* designs, a 2-layer primary should be used. The resultant increase in the intra-winding capacitance limits the peak drain voltage at turn off. For output powers greater than 2 W, the winding capacitance is not sufficient to limit peak drain voltage. Therefore a bias winding should be added to the transformer and rectified with a standard recovery (rectifier) diode. Suitable diodes for the bias winding include 1N4003–1N4007. The addition of a bias winding acts as a clamp and also reduces leakage inductance ringing and improves EMI. Table 6 summarizes the requirements between *Clampless* designs and designs using an external clamp.

Clampless designs should only be attempted with the LNK362 device. The higher current limit of the larger family members make it impractical to limit the peak drain voltage without an external clamp.

For output powers > 2.5 W, either an RCD or Zener clamp is suggested. Select the initial clamp components using Table

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	IR
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	IR/On Semi
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
MUR110 to MUR160	Ultrafast	100-600	1	Leaded	On Semi
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay

Table 8. List of Recommended Diodes That May Be Used With LinkSwitch-XT Designs.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			6.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.33	Amps	Output DC Current
PO1			2.00	Watts	Output Power
VD1			0.50	Volts	Output Diode Forward Voltage Drop
NS1			11.00		Output Winding Number of Turns
ISRMS1			0.68	Amps	Output Winding RMS Current
IRIPPLE1			0.60	Amps	Output Capacitor RMS Ripple Current
PIVS1			36.45	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			UF4001, SB150		Recommended Diodes for this output
Pre-Load Resistor			2	k-Ohms	Recommended value of pre-load resistor
CMS1			136.99	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			28.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.32	mm	Minimum Bare Conductor Diameter
ODS1			0.76	mm	Maximum Outside Diameter for Triple Insulated Wire

Figure 7. Secondary Design Parameters. Includes a Recommended Diode Part.

as guide. If an RCD clamp is selected, then some empirical adjustment of the values is normally required to take account of the actual V_{OR} and transformer leakage inductance of the design. As a general rule, minimize the value of the capacitor and maximize the value of the resistor. For both RCD and Zener clamps, verify that the peak drain voltage does not exceed 650 V at the highest input voltage and peak (overload) output power.

Step 8 – Selection of Output Diode and Pre-Load Resistor

$V_R \geq 1.25 \cdot PIVS$, where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters.

$I_D \geq 2 \cdot I_O$, where I_D the diode rated DC current and I_O is the output current.

Additionally, Table 8 lists some of the suitable Schottky and ultra-fast diodes that may be use with *LinkSwitch-XT* circuits. The *LinkSwitch-XT* spreadsheet also recommends a diode based on the above guidelines (see Figure 7).

Select the pre-load resistor such that it will sink 3 mA at the specified voltage. Note that a pre-load resistor also increases the no-load losses, so verify acceptable no-load consumption.

Step 9 – Selection of Output Capacitors

Ripple Current Rating

Select the output capacitor(s) such that the ripple rating is greater than the calculated value, I_{RIPPLE} from the spreadsheet.

Many capacitor manufacturers provide factors that increased the allowable ripple current as the capacitor temperature is reduced or the frequency of the ripple is increased from the

Output Type	CV/CC	CV Only
Suggested Feedback		
Notes	$R_{SENSE} = V_{F(UFB)} / I_O$ $VR_{FB} = V_O - V_{BE(QFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) $R_B = V_{BE(QFB)} / I_{ZT(VRFB)}$ R_A : Limits base-emitter current of Q_{FB} R_C and R_D : Limits U_{FB} current U_{FB} : Use high CTR device (200% - 600%) Q_{FB} : Any small signal PNP transistor (Values shown for a 5.5 V, 500 mA output)	$VR_{FB} = V_O - V_{F(UFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) $R_B = V_{BE(QFB)} / I_{ZT(VRFB)}$ R_A : Limits U_{FB} current during transients and allows small output voltage adjustments. U_{FB} : Use high CTR device (200% - 600%) L_A : Optional for lower output switching noise (Use ferrite bead or low value (1-3 μ H) inductor rated for I_O) C_A : Optional for lower output switching noise (Use low ESR, 100 μ F with voltage rating $> 1.25 \cdot V_O$) (Values shown are for a 5 V output)

Table 9. Examples of Feedback Configurations.

data sheet specified values. This should be considered to ensure the capacitor is not oversized, increasing the cost. Two or more capacitors may be used in parallel to give a combined ripple current rating equal to the sum of the individual capacitor ratings.

ESR specification

Select a low ESR type, which gives acceptable output switching ripple. The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. Generally the selection of the capacitor for ripple current rating will also result in an acceptable ESR.

Voltage Rating

Select a voltage rating such that $V_{RATED} \geq 1.25 \cdot V_O$.

Step 10 – Choose Feedback Scheme and Select Feedback Components

Two separate feedback schemes are recommended with the *LinkSwitch-XT*. The first is primary-side regulated feedback (also called bias winding feedback), shown in Figure 9. This scheme relies on the bias winding to regulate the output voltage. The bias winding voltage is divided down by a resistor divider such that the feedback pin is 1.65 V at the specified output voltage. The output voltage is then regulated through the turns ratio of the secondary and bias windings.

In bias winding feedback, the bias winding may be placed closer to the secondary winding for tighter coupling and thus better regulation or it may be placed away from the secondary winding for loose regulation of output voltage. Bias winding

Figure 11 shows the factors to be considered while deciding the mechanical structure of the transformer.

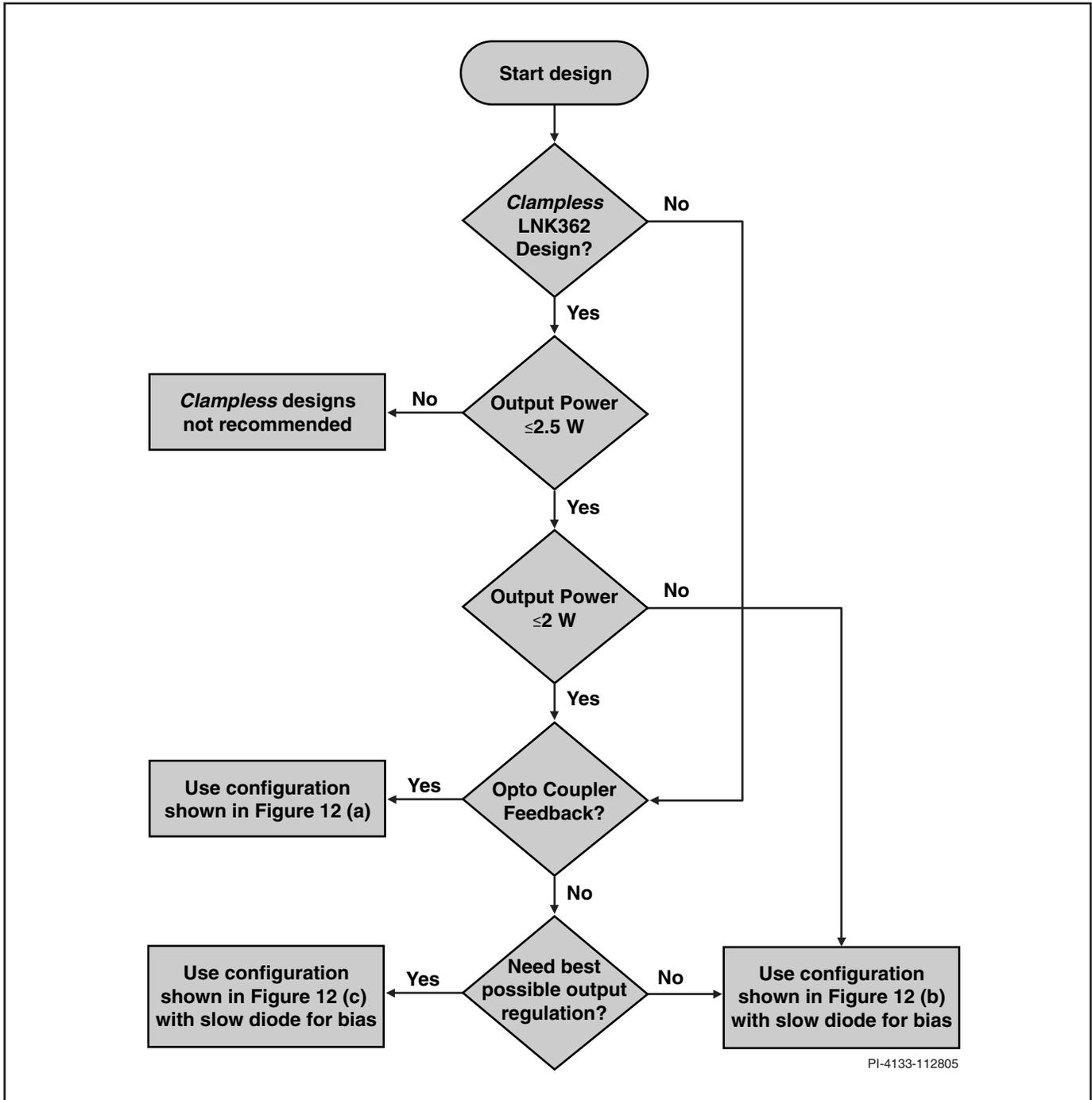


Figure 11. Flowchart For Deciding Mechanical Structure of Transformer.

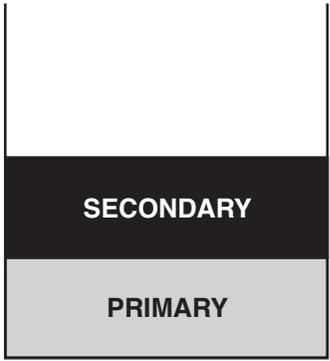
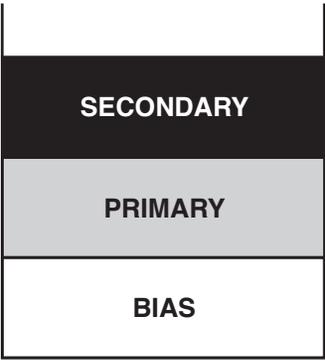
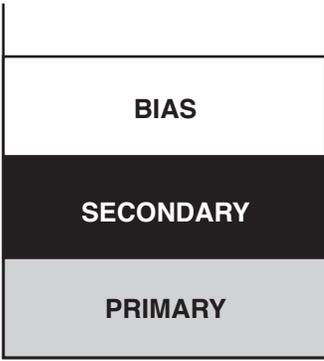
 <p style="text-align: center;">(a)</p>	 <p style="text-align: center;">(b)</p>	 <p style="text-align: center;">(c)</p>
<ul style="list-style-type: none"> • No bias winding • For <i>Clampless</i> designs use 2 primary layers, LNK362 and ≤ 2 W only 	<ul style="list-style-type: none"> • For <i>Clampless</i> LNK362 designs and ≤ 2.5 W only • Bias winding feedback ideal for designs that require loosely regulated output voltage • Improved EMI performance over (a) & (c) due to reduction in leakage inductance ringing 	<ul style="list-style-type: none"> • For <i>Clampless</i> LNK362 designs, 2 primary layers and ≤ 2 W only • Provides best output voltage regulation with bias winding feedback

Figure 12. Mechanical Structure of the Transformer in LinkSwitch-XT Designs.

Notes



Notes

Revision	Notes	Date
A	-	11/05
B	Formatting	11/05

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