TOPSwitch® Flyback Design Methodology

Application Note AN-16

Designing an off-line switching power supply involves many aspects of electrical engineering: analog and digital circuits, bipolar and MOS power device characteristics, magnetics, thermal considerations, safety requirements, control loop stability, etc. This presents an enormous challenge involving complex trade-offs with a large number of design variables. However, with *TOPSwitch*'s high level of integration, this design task has been greatly simplified. Because of the significantly reduced number of design variables and built-in loop stability, it is possible to develop a simple step-by-step design method that is easy to follow and quickly leads to satisfactory results.

Introduction

The design of a switching power supply, by nature, is an iterative process with many variables that have to be adjusted to optimize the design. The design method described below consists of three parts: a complete design flow chart, a simplified step-by-step design procedure and an in-depth information section. The flow chart, at conceptual level, serves as a map providing an overall picture and guideline for the complete design methodology. The step-by-step design procedure is a simplified version of the design method which, at implementation level, guides the reader from a set of given system requirements/ specifications all the way to the completion of the desired *TOPSwitch* flyback power supply using rules of thumb, look up tables and a simple spread sheet program. The information section, at optimization level, makes available the key background information for the design method, such as equations and guidelines. Cross references are provided among the three which allow the reader to switch among conceptual, implementation and optimization levels at any given stage for an in-depth understanding and/or further optimization.

Basic circuit configuration

Because of the high level integration of *TOPSwitch*, many power supply design issues are resolved in the chip. Far fewer issues are left to be addressed externally, resulting in one basic circuit configuration remaining unchanged from application to application. Different output power levels may require the use of different values for some circuit components, but the circuit configuration itself stays valid. Application specific issues outside of the basic flyback converter requirements (such as constant current, constant power outputs, etc.) are beyond the

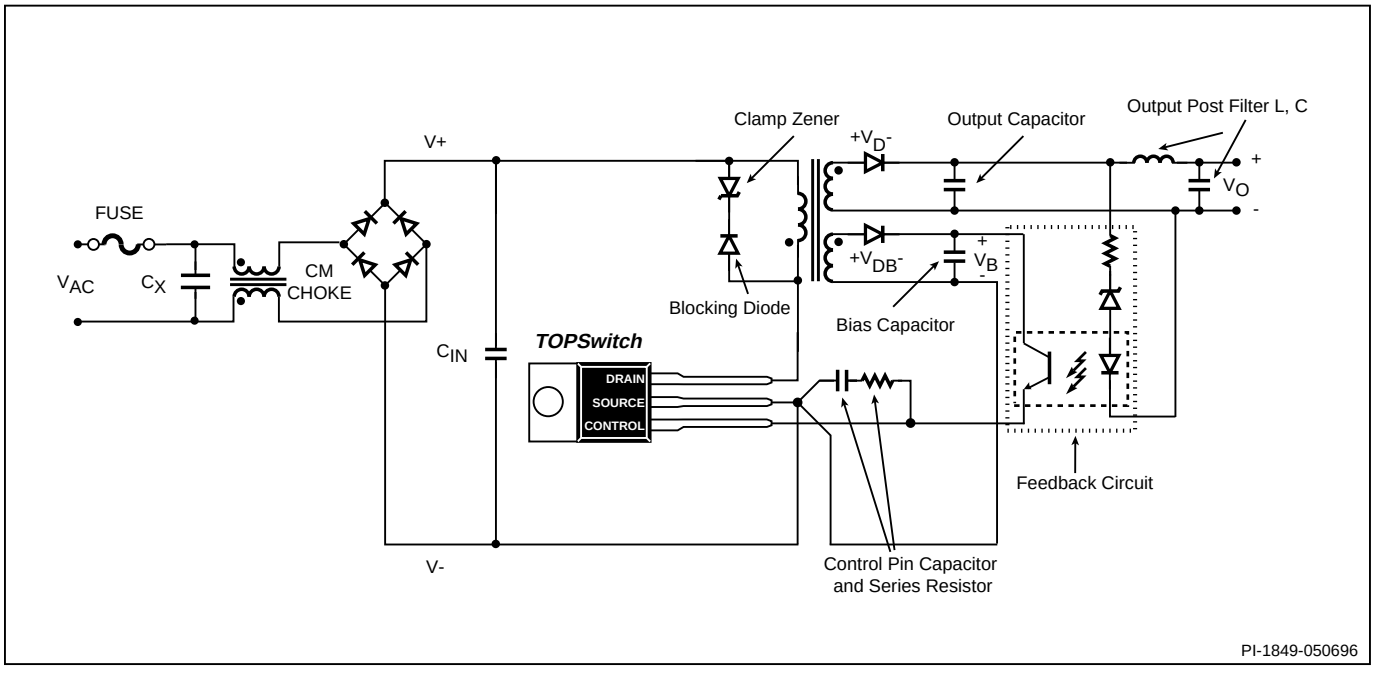

Figure 1. Typical TOPSwitch Flyback Power Supply.

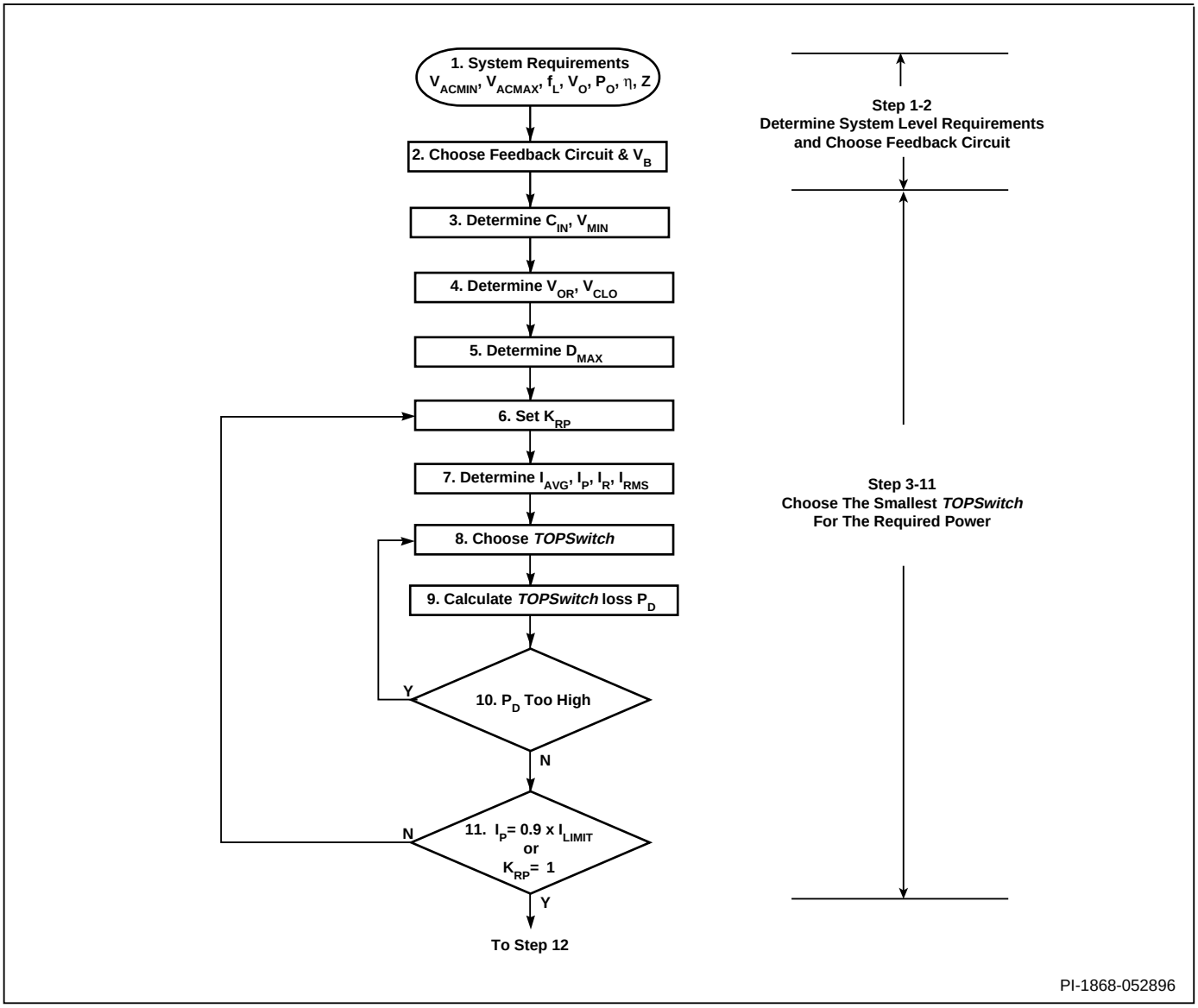

Figure 2A. TOPSwitch Flyback Design Flow Chart, Step 1 to 11.

scope of this application note. However, such requirements are usually implemented by adding additional circuitry to the basic converter configuration. The only part of the circuit configuration that may change is the feedback circuitry. Depending on the power supply output requirement, one of four possible circuits, shown in Figures 3-6, will be chosen for the application.

The basic circuit configuration used in most *TOPSwitch* flyback power supplies is shown in Figure 1 which also serves as the reference circuit for component identifications used in the descriptions throughout this application note.

Design Flow

Figure 2A, B and C present a design flow chart showing the complete design procedure in 35 steps. With the basic circuit configuration shown in Figure 1 as its foundation, the logic behind this design approach can be summarized as following:

1. Determine system requirements and decide on feedback circuit accordingly.
2. Find the smallest *TOPSwitch* capable for the application.
3. Design the smallest transformer for the *TOPSwitch* chosen.
4. Select all other components in Figure 1 to complete the design.

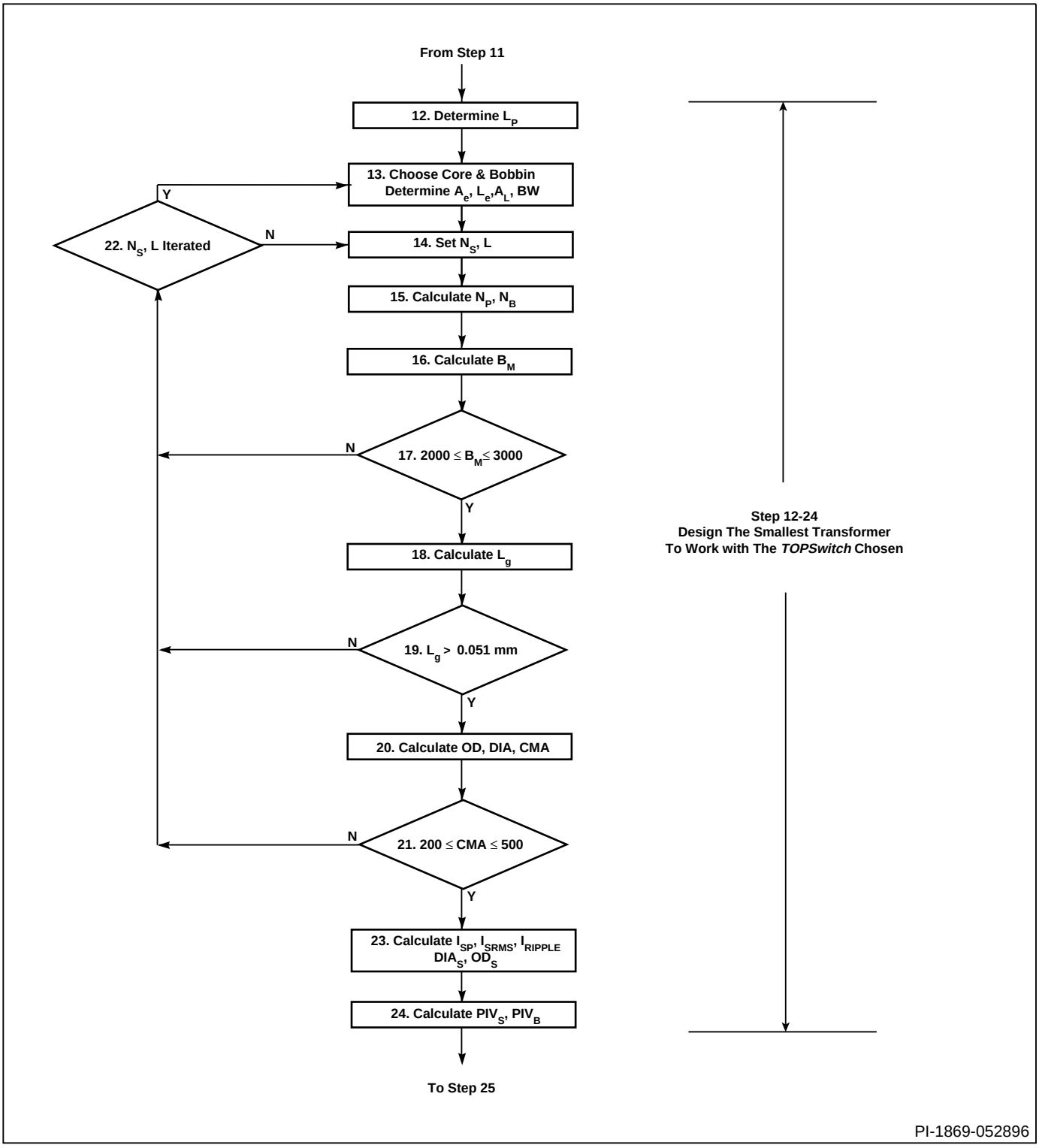

Figure 2B. TOPSwitch Flyback Design Flow Chart, Step 12 to 24.

The overriding objective of this procedure is “design for cost effectiveness”. Using smaller components will usually lead to a less expensive power supply. However, for applications with stringent size or weight limitations, the designer may need to strike a compromise between cost and specific design requirements in order to achieve the ultimate cost effectiveness at the end product.

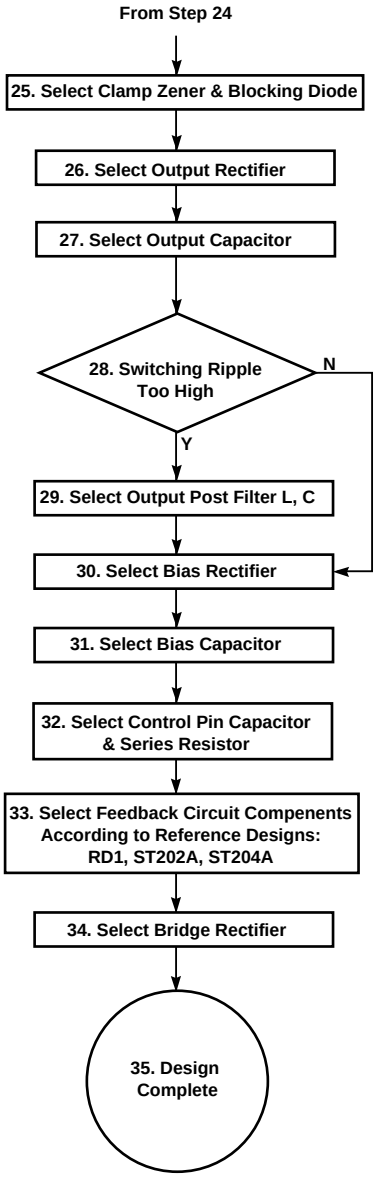

Figure 2C. TOPSwitch Flyback Design Flow Chart, Step 25 to 35.

Step by Step Design Procedure

This design procedure uses the AN-17 spreadsheet (available from Power Integrations), which contains all the important equations required for a *TOPSwitch* flyback power supply design, and automates most calculations. Designers therefore are relieved from the tedious calculations involved in the complicated and highly iterative design process. Anytime a parameter is involved in a calculation, whether it is an input or an output, a cell location for the parameter will be shown in parenthesis at the right side of the page. For example (A1) denotes column A and row 1. Note that all user provided inputs are in column B and all spreadsheet calculated results are in column D. Column C is reserved for intermediate variables needed in some complicated calculations. Look up tables and rules of thumb are also provided wherever appropriate, to facilitate the design task. For questions regarding any particular step of this procedure, please refer to the corresponding step in the information section, where in-depth explanation is provided.

Step 1.
Determine system requirements: V_{ACMAX}, V_{ACMIN}, f_L, f_S, V_O, P_O, η, Z

- Set minimum AC input voltage, V_{ACMIN}, per Table 1 (B3)
- Set maximum AC input voltage, V_{ACMAX}, per Table 1 (B4)

Input (VAC)	V_{ACMIN} (VAC)	V_{ACMAX} (VAC)
100/115	85	132
Universal	85	265
230	195	265

Table 1

- Line frequency, f_L: 50Hz or 60Hz (B5)
- *TOPSwitch* switching frequency, f_S: 100KHz (B6)
- Output voltage, V_O: in Volts (B7)
- Output power, P_O: in Watts (B8)
- Power supply efficiency, η: 0.8 if no better reference data available (B9)
- Loss allocation factor, Z: 0.5 if no better reference data available (B10)

Step 2.
Choose feedback circuit and bias voltage V_B based on output requirements:

- Select a feedback circuit (Figures 3-6) based on output specification:

Feedback Circuit	V_B (V)	Output Accuracy	Load Regulation	Line Regulation	Reference Design
Primary/basic	5.7	±10%	±5%	±1.5%	RD1
Primary/enhanced	27.7	±5%	±2.5%	±1.5%	RD1
Opto/Zener	12	±5%	±1%	±0.5%	ST202A
Opto/TL431	12	±1%	±0.2%	±0.2%	ST204A

Table 2

- Choose required bias voltage, V_B , per Table 2 (B11)

Step 3.
Determine input storage capacitor C_{IN} and minimum DC input voltage V_{MIN} based on input voltage and P_O:

- Set bridge rectifier conduction time, t_C = 3 mS (B12)
- Choose input storage capacitor, C_{IN}, per Table 3 (B13)
- Derive minimum DC input voltage, V_{MIN} (D33)

Input (VAC)	C_{IN} (µF/Watt of P_O)	V_{MIN} (V)
100/115	2~3	≥90
Universal	2~3	≥90
230	1	≥240

Table 3

Step 4.
Determine reflected output voltage V_{OR} and clamp Zener voltage V_{CLO} based on input voltage:

- Set V_{OR} based on input voltages per Table 4 (B16)

Input (VAC)	V_{OR} (V)	V_{CLO} (V)
100/115	60	90
Universal	135	200
230	135	200

Table 4

Note : V_{CLO} is to be used in Step 25 for clamp Zener selection

Step 5.
Determine D_{MAX} based on V_{MIN} and V_{OR}:

- Set *TOPSwitch* Drain to Source voltage, V_{DS} = 10 V (B17)
- Determine maximum duty cycle at low line, D_{MAX} (D37)

Step 6.
Set value for primary ripple current I_R to primary peak current I_P ratio, K_{RP}:

- Starting with: K_{RP} = 0.4 for 100/115 VAC or universal input (B20)
  0.6 for 230 VAC
- K_{RP} must be kept within the range specified in Table 5 throughout iteration

Input (VAC)	K_{RP}	
	Minimum (Most Continuous)	Maximum (Discontinuous)
100/115	0.4	1.0
Universal	0.4	1.0
230	0.6	1.0

Table 5

Step 7.
Determine primary waveform parameters I_{AVG}, I_P, I_R, I_{RMS}:

- Calculate average input current, I_{AVG} : in Amps (D38)
- Calculate primary Peak current, I_P: in Amps (D39)
- Calculate primary ripple current, I_R: in Amps (D40)
- Calculate primary RMS current, I_{RMS} : in Amps (D41)

Step 8 to Step 10.
Choose the smallest possible *TOPSwitch* for the job under practical thermal limitation

- Start with the smallest *TOPSwitch* based on minimum current limit spec such that 0.9 x I_{LIMIT}(minimum) ≥ I_P
- Refer to AN-14 Table 2 for thermal considerations. Select larger *TOPSwitch* if necessary.

Step 11.
Check minimum I_{LIMIT} of the selected *TOPSwitch* against required peak current I_P. Increase K_{RP} until K_{RP} = 1.0 or I_P = 0.9 x I_{LIMIT}(minimum)

- Enter new value of K_{RP} (B20)
- Monitor I_P (D39)
- Iterate until K_{RP} = 1.0 or I_P = 0.9 x I_{LIMIT}(minimum)

Step 12.
Calculate primary inductance L_P (D44)

Step 13.
Choose core and bobbin based on P_O using AN-18 Appendix A, Table 2 and determine A_e, L_e, A_L and BW from core and bobbin catalog:

- Core effective cross sectional area, A_e: in cm^2 (B24)
- Core effective path length, L_e: in cm (B25)
- Core ungapped effective inductance, A_L: in $nH/turn^2$ (B26)
- Bobbin width, BW : in mm (B27)

Step 14.
Set value for number of primary layers L and number of secondary turns N_S (may need iteration):

- Starting with L = 2 (Keep 1.0 ≤ L ≤ 2.0 throughout iteration) (B29)
- Starting with N_S= 1 turn/volt for 100/115 VAC (B30)
  0.6 turn/volt for 230 VAC and universal inputs
- Both L and N_S may need iteration

Step 15.
Calculate number of primary turns N_P and number of bias turns N_B:

- Diode voltages: use 0.7V for P/N diode and 0.4V for schottky diode
- Set output rectifier forward voltage, V_D (B18)
- Set bias rectifier forward voltage, V_{DB} (B19)
- Calculate number of primary turns N_P (D45)
- Calculate number of bias turns N_B (D46)

Step 16 to Step 22.
Check B_M, CMA and L_g. Iterate if necessary by changing L, N_S or core/bobbin until within specified range:

- Set safety margin, M. Use 3 mm (118 mils) for margin wound with 230 VAC or universal input and 1.5 mm (59 mils) for 110/115 VAC input. Set to zero for triple insulated secondary. (B28)
- Maximum flux density, B_M: $3000 \geq B_M \geq 2000$; in Gauss (D48)
- Gap length, L_g: $L_g \geq 0.051$ mm (D51)
- Primary winding current capacity, CMA: $500 \geq CMA \geq 200$; in circular mils per Amp (D58)
- Iterate by changing L, N_S, core/bobbin according to Table 6
- Primary minimum conductor diameter, DIA: in mm (D55)
- Primary maximum wire outside diameter, OD: in mm (D53)

		B_M	L_g	CMA
L	↑	-	-	↑
N_S	↑	↓	↑	↓
Core	↑	↓	↑	↑

(B29)
(B30)
(B24/25/26/27)

Table 6

Step 23.
Determine secondary parameters I_{SP}, I_{SRMS}, I_{RIPPLE}, DIA_S, OD_S:

- Secondary Peak current, I_{SP}: in Amps (D61)
- Secondary RMS current, I_{SRMS}: in Amps (D62)
- Output capacitor ripple current, I_{RIPPLE}: in Amps (D64)
- Secondary minimum conductor diameter, DIA_S: in mm (D68)
- Secondary maximum wire outside diameter, OD_S: in mm (D69)

Step 24.
Determine maximum peak inverse voltages PIV_S, PIV_B for secondary and bias windings:

- Secondary winding maximum peak inverse voltage PIV_S: in Volts (D74)
- Bias winding maximum peak inverse voltage PIV_B: in Volts (D75)

Step 25.
Select clamp Zener and blocking diode for primary clamping per Table 7 based on input voltage and V_{CLO} (from Step 4):

Input (VAC)	V_{CLO} (V)	Zener	Diode
100/115	90	P6KE91	BYV26B
Universal	200	P6KE200	BYV26C
230	200	P6KE200	BYV26C

Table 7

Notes: 1. P6KE91: 91V/5W; Motorola
P6KE200: 200V/5W; Motorola
BYV26B: 400V/1A, UFR; Philips
BYV26C: 600V/1A, UFR; Philips
2. Ishizuka 180V Zener may be used for lower power TOP210, TOP200, TOP201 applications

Step 26.
Select output rectifier per Table 8 such that:

- $V_R \geq 1.25 \times PIV_S$; where PIV_S is from Step 24 and V_R is the rated reverse voltage of the rectifier diode
- $I_D \geq 3 \times I_O$; where I_D is the diode rated DC current and $I_O = P_O/V_O$

Rectifier Diode		V_R (V)	I_D (A)	Manufacturer
Schottky	1N5819	40	1.0	Motorola
	1N5822	40	3.0	Motorola
	MBR745	45	7.5	Motorola
	MBR1045	45	10	Motorola
	MBR1645	45	16	Motorola
UFR	UF4002	100	1.0	GI
	MUR110	100	1.0	Motorola
	MUR120	200	1.0	Motorola
	UF4003	200	1.0	GI
	BYV27-200	200	2.0	Philips, GI
	UF5401	100	3.0	GI
	UF5402	200	3.0	GI
	MUR410	100	4.0	Motorola
	MUR420	200	4.0	Motorola
	MUR810	100	8.0	Motorola
	MUR820	200	8.0	Motorola
	BYW29-200	200	8.0	Philips, GI
	BYV32-200	200	20	Philips

Table 8

Step 27.
Select output capacitor based on I_{RIPPLE} (from Step 23):

- Capacitor ripple current specified @ 105 ^{O}C, 100KHz must be equal or larger than $I_{RIPPLE,}$ where I_{RIPPLE} is from Step 23.
- Use low ESR, electrolytic capacitor. Output switching ripple voltage is I_{SP} x ESR , where I_{SP} is from Step 23.
- Use parallel capacitors to increase ripple current capacity for high current outputs.
- Examples:

Output	Output Capacitor
5V to 24V, 1A	330uF, 35V, low ESR, electrolytic United Chemicon LXF35VB331M10X20LL Nichicon UPL1V331MRH Panasonic ECA-1VFQ331L
5V to 24V, 2A	1000uF, 35V, low ESR, electrolytic UnitedChemicon LXF35VB102M12.5X30LL Nichicon UPL1V102MRH Panasonic ECA-1VFQ102L

Step 28. to Step 29.
Add output LC post filter if and only if output switching ripple voltage is not within specification:

- Inductor L: 2.2 to 4.7µH. Use ferrite bead for low current (≤ 1A) output and standard off the shelf choke for higher current output. Increase choke current rating or wire size if necessary to avoid significant DC voltage drop.
- Capacitor, C: 120uF, 35V, low ESR electrolytic
  United Chemicon LXF35VB121M8X12LL
  Nichicon UPL1V121MRH
  Panasonic ECA-1VFQ121L

Step 30.
Select bias rectifier per Table 9 such that $V_R \geq 1.25 \times PIV_B$; where PIV_B is from Step 24 and V_R is the rated reverse voltage of the rectifier diode.

Rectifier	V_R(V)	Manufacturer
1N4148	75	Motorola
BAV21	200	Philips
UF4003	200	GI

Table 9

Step 31.
Select bias capacitor:

- Use 0.1uF, 50V, ceramic

Step 32.
Select Control pin capacitor and series resistor:

- Control pin capacitor: use 47uF, 10V, low cost electrolytic (Do not use low ESR capacitor).
- Series resistor: use 6.2 Ω, 1/4 Watt (Not needed if $K_{RP} = 1$, e.g. discontinuous mode).

Step 33.
Select feedback circuit components according to applicable Reference Design: RD1, ST202A, ST204A.

- Applicable reference design: identified in Step 2.
- Detailed component information: refer to appropriate reference design board documentation.

Step 34.
Select input bridge rectifier such that:

- $V_R \geq 1.25 \times (1.414 \times V_{ACMAX})$; where V_{ACMAX} is from Step 1.
- $I_{ACRMS} \geq 2 \times I_D$; where I_D is the bridge rectifier rated RMS current and I_{ACRMS} is the input RMS current.

Note: $I_{ACRMS} = \dfrac{P_O}{\eta \times V_{ACMIN} \times PF}$; where V_{ACMIN} is from step 1 and PF is the power factor of the power supply which is typically between 0.5 and 0.7. If no better reference data is available, use 0.5.

Step 35. *TOPSwitch* flyback power supply design complete.

In-depth Information

Step 1. Determine system requirements: V_{ACMAX}, V_{ACMIN}, f_L, f_S, V_O, P_O, η, Z

The step-by-step procedure uses predetermined parameter values such as V_{ACMAX}, V_{ACMIN}, V_{MIN}, V_{OR} and V_{CLO} for most commonly encountered input voltage ranges: 85 to 132 VAC for 100/115 VAC, 195 to 265 VAC for 230 VAC and 85 to 265 VAC for universal input. A ±15% line voltage variation is assumed in all cases. Applications with a different input voltage range can be handled by following the information and methods provided in Step 3, 4 and 5 of this in-depth information section to derive appropriate values for C_{IN}, V_{OR}, V_{CLO} and V_{MIN}.

Efficiency η is the ratio of output power to input power. Since efficiency can vary significantly with output voltage due to secondary diode loss, it is best to use a number that is representative of similar power supplies. Switching power supply efficiencies typically range from 75% for supplies delivering most of their power at low voltage outputs (5 or 3.3V) to 85% for those supplying most of their power through higher voltage outputs (12V and above). If this data is not available, 80% is a reasonable choice.

For a power supply with an output power P_O and an efficiency η, P_O x (1-η)/η watts of power is lost somewhere in the system: part in the secondary circuits, and the balance in the primary circuits. It is important to know the loss distribution between primary and secondary because only the secondary losses represent power that must be processed by the transformer and considered in the transformer design. Note that the power dissipated at the primary clamp is considered as secondary loss because this power is processed by the transformer before being delivered to the clamp circuit. The ratio of the secondary loss to the total loss is defined as the loss allocation factor, Z, which should be set based on experience. A value of 0.5 should be used if no reference data is available.

Step 2. Decide on a Feedback/sense circuit and bias voltage V_B

Four types of feedback/sense circuits are recommended. The primary feedback circuit, shown in Figure 3, is the least expensive but has lower absolute accuracy and regulation and is suitable only for low power and higher output voltage (V_O >5V). Output accuracy can be improved for the primary feedback circuit by adding a 22V Zener and a capacitor as shown in Figure 4. The

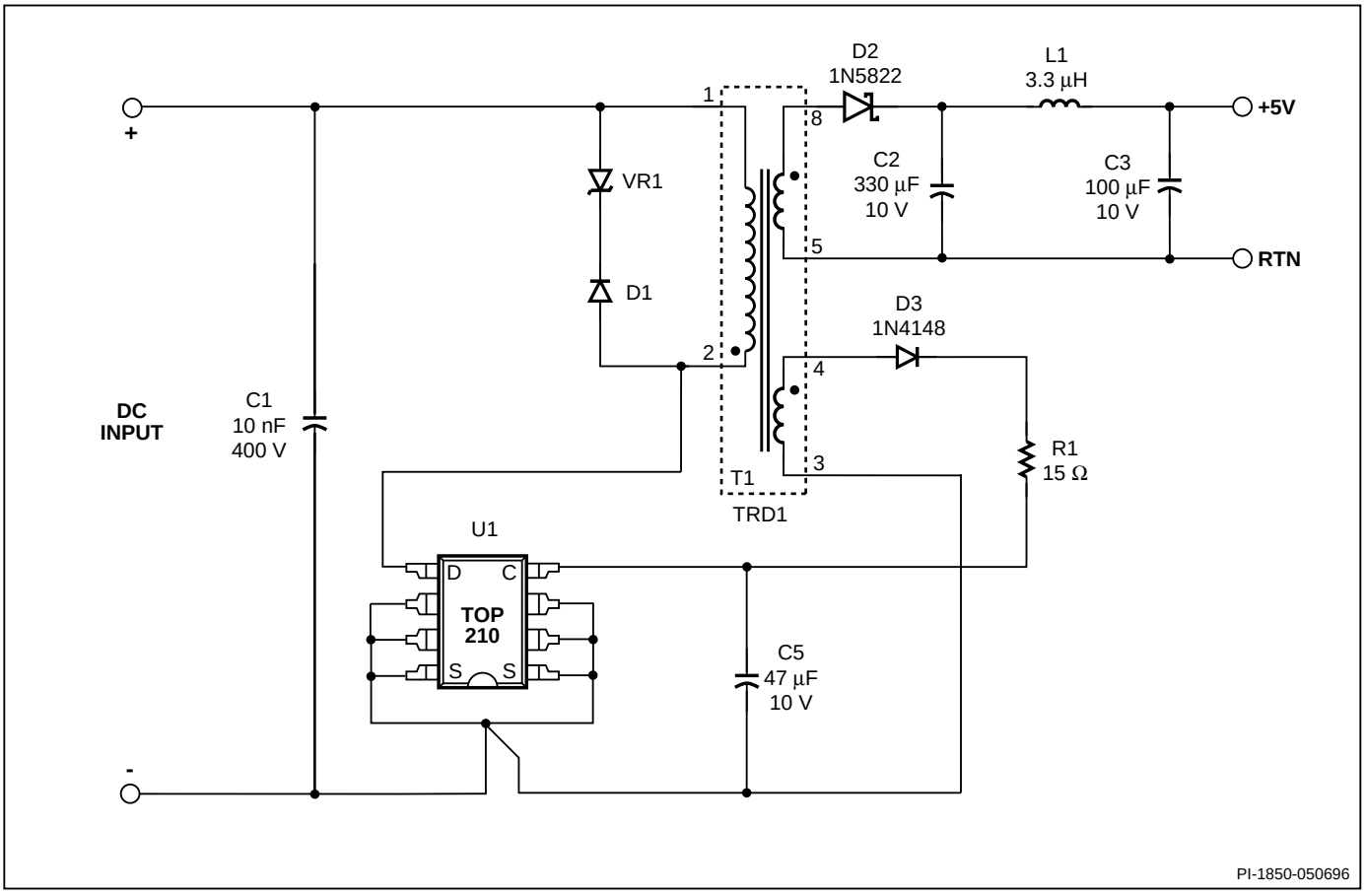

Figure 3. RD1 Reference Design Board.

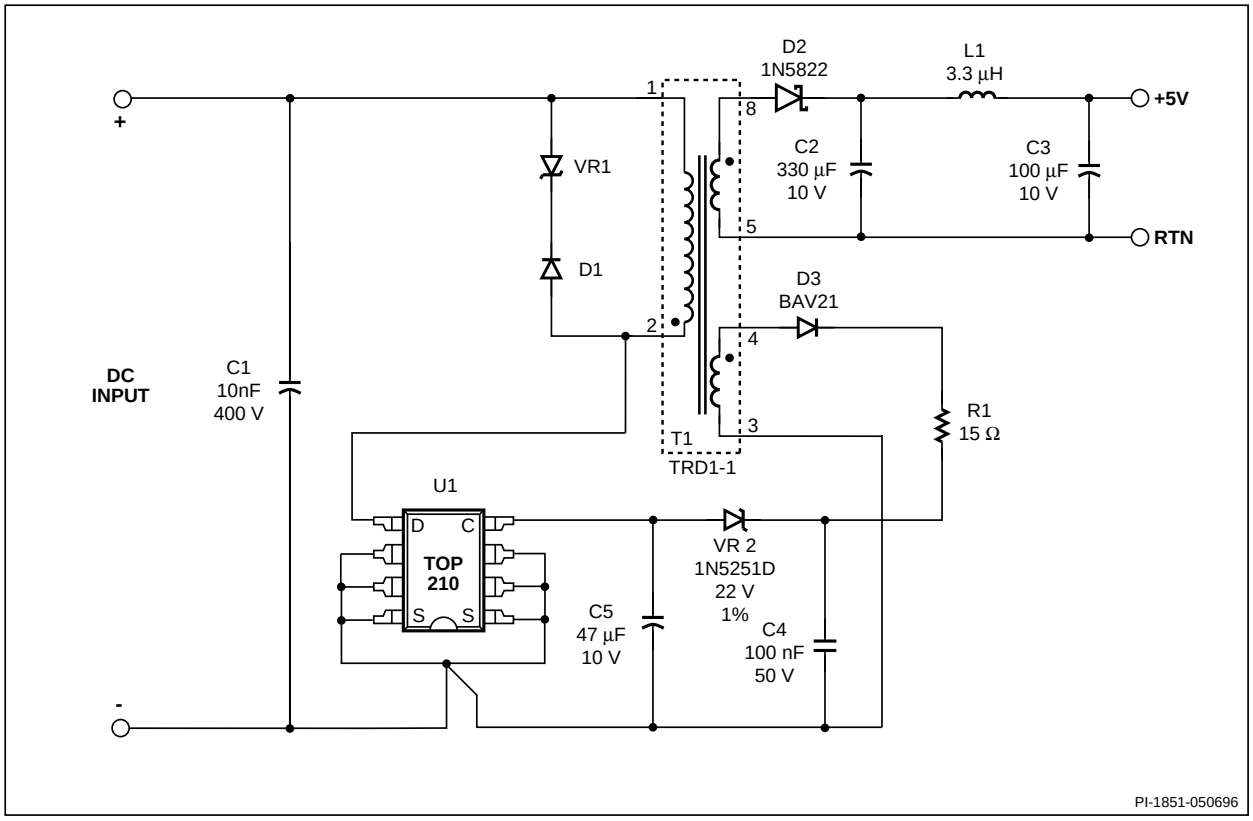

Figure 4. RD1 Reference Design Board (Enhanced).

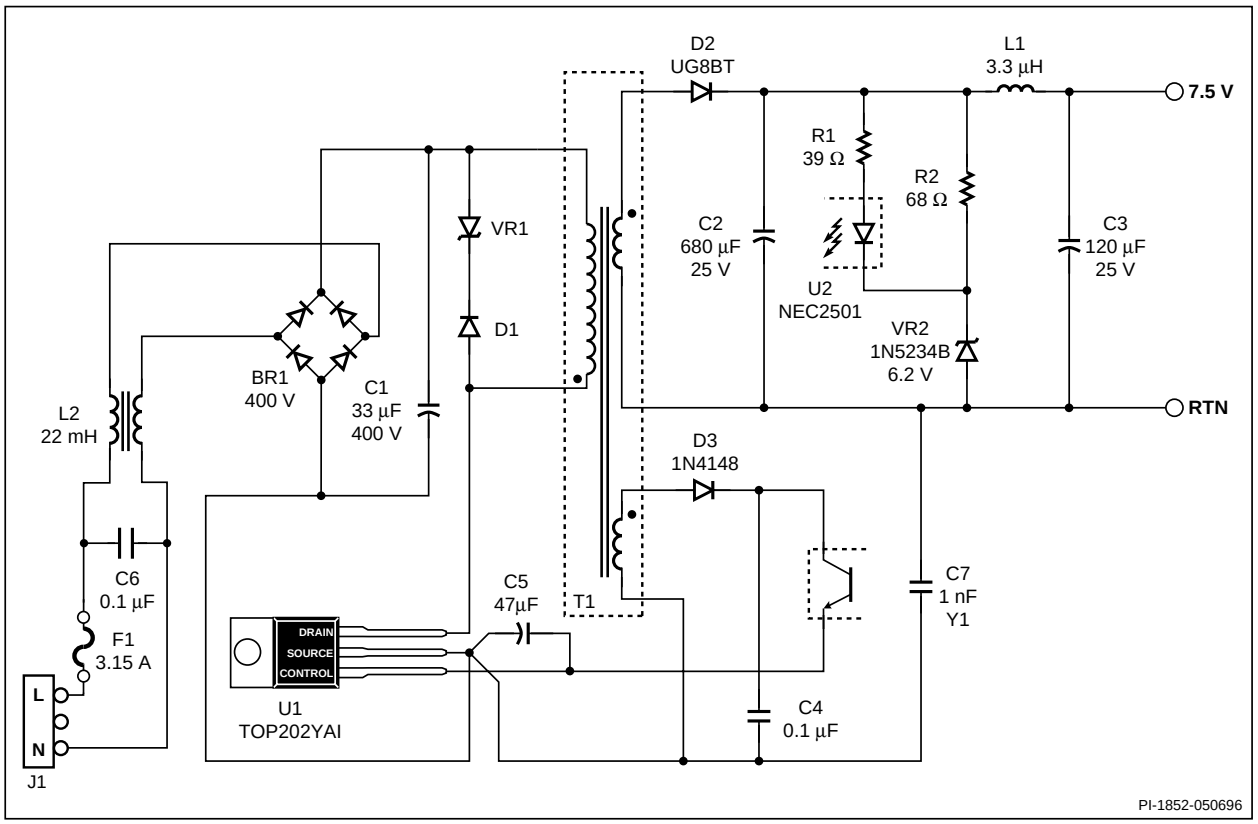

Figure 5. ST202A Reference Design Board.

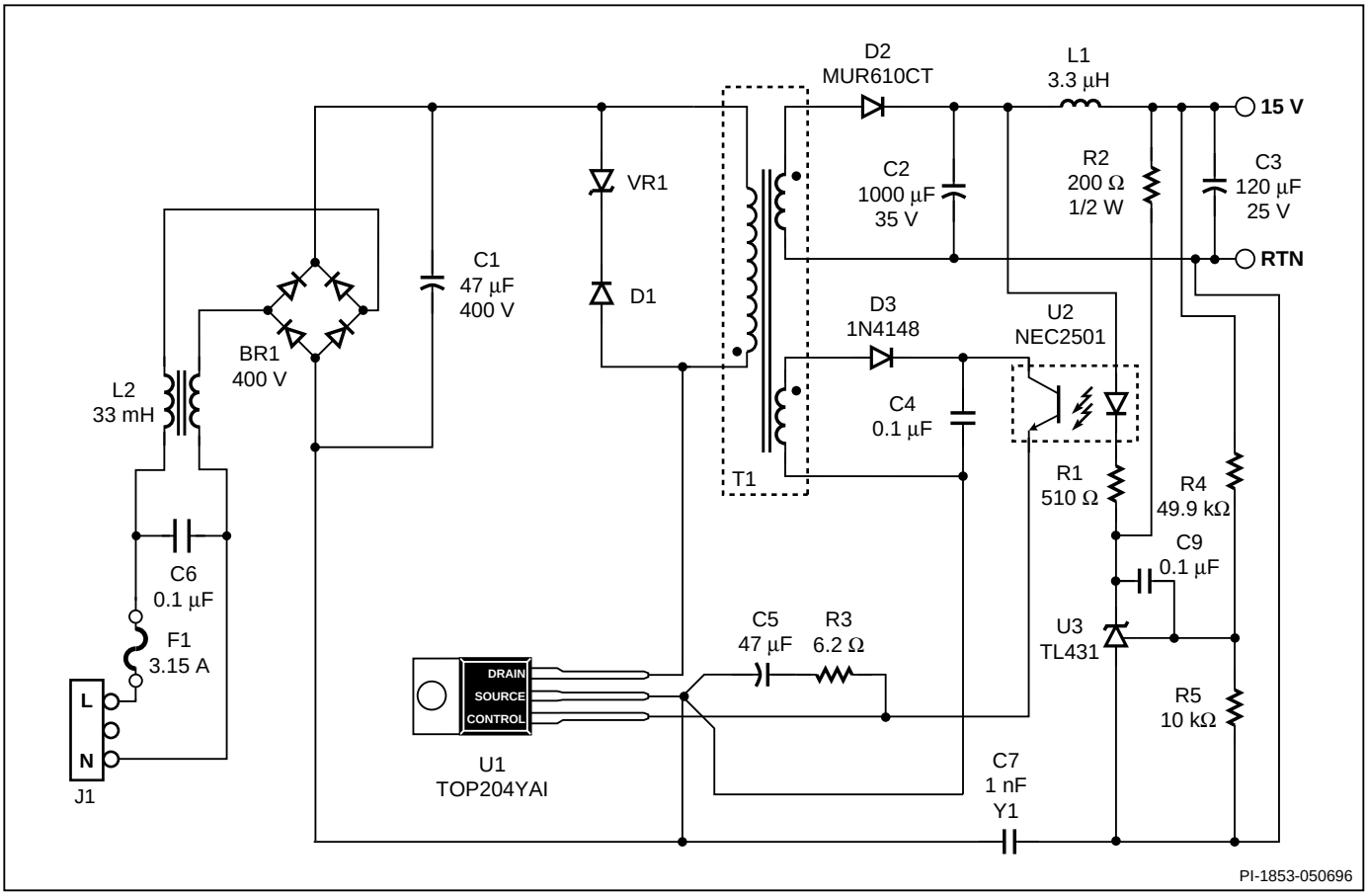

Figure 6. ST204A Reference Design Board.

opto-coupler feedback using an accurate reference/comparator (Figure 6) such as the TL431 for sensing provides high accuracy and regulation at a slightly added cost and is applicable to all power and voltage ranges. An intermediate solution is to use an opto-coupler with a Zener sense circuit (Figure 5). This technique is suitable for medium power levels (up to 30W) and is reasonably accurate, especially at output voltages higher than 5V.

Step 3. Determine input capacitor C_{IN} and minimum DC input voltage V_{MIN}

When the full wave rectified AC line is filtered with an input capacitance C_{IN} (Figure 1), the resulting High Voltage DC bus (V+) has a ripple voltage as shown in Figure 7. The minimum DC voltage V_{MIN} occurring at the lowest line voltage V_{ACMIN} is an important parameter for the design of the power supply. A rule of thumb on choosing the C_{IN} value is to use 2 to 3 µF per watt of output power for 100/115 VAC or universal input, and 1 µF/Watt for 230VAC. This results in a V_{MIN} of 90VDC for 100/115VAC or universal input and 240VDC for 230VAC, respectively. The C_{IN} value obtained by using this rule represents a nearly optimum design in terms of system cost in most applications. Higher values of C_{IN} increase capacitor cost without a corresponding pay back in terms of higher V_{MIN} or lower ripple, whereas lower values of C_{IN} result in significantly lower V_{MIN} increasing *TOPSwitch* cost due to increased peak operating current demand. Lower values of C_{IN} also increase input ripple voltage, which could increase output ripple voltage if the control loop gain is a limiting factor.

The accurate calculation of V_{MIN} for a given C_{IN} (or vice versa) is a very complicated task which involves the solving of an equation with no closed form solution. The equation shown below represents a good first order approximation which is accurate enough for most situations.

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}^2) - \frac{2 \times P_O \times \left(\frac{1}{2 \times f_L} - t_C \right)}{\eta \times C_{IN}}}$$

t_C is typically 3 ms, and can be verified by direct measurement.

Step 4. Determine reflected output voltage V_{OR} and clamp Zener voltage V_{CLO}:

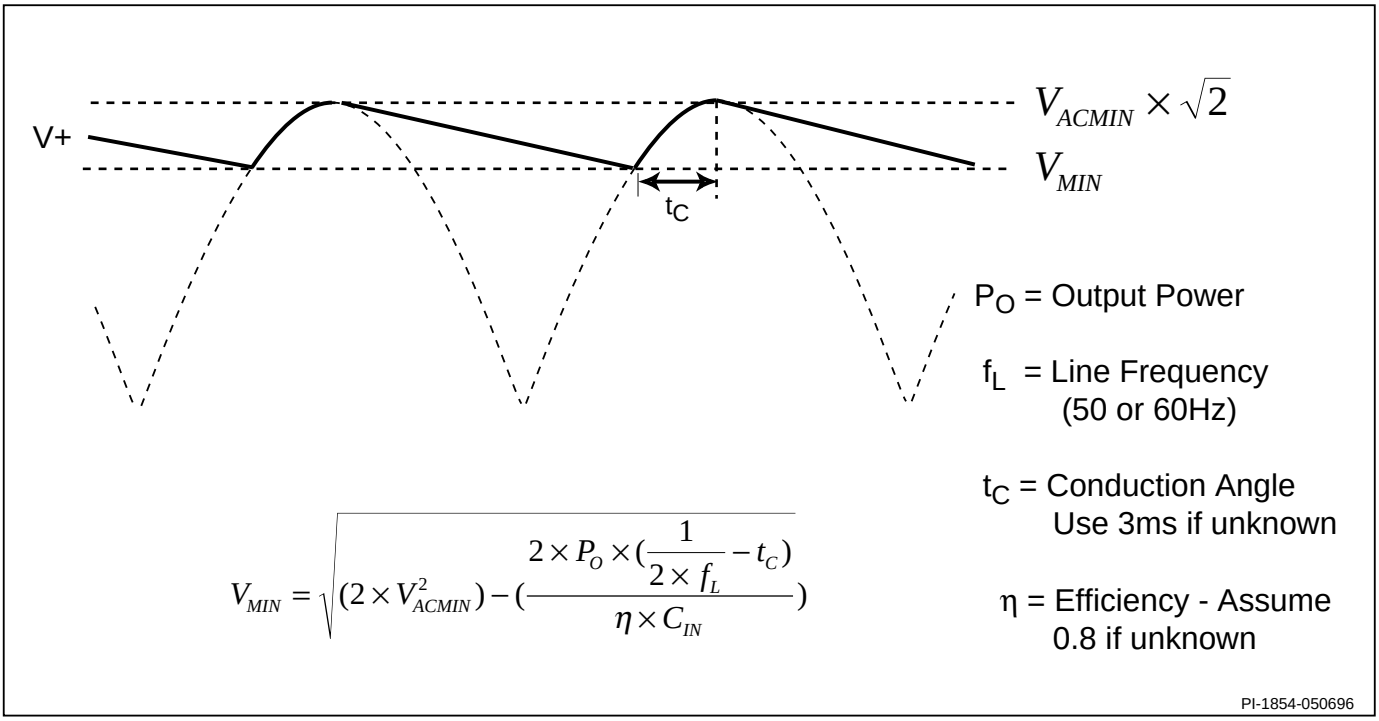

Figure 7. Input Voltage Waveform.

A typical flyback circuit using *TOPSwitch* is shown in Figure 1. When the *TOPSwitch* is off and the secondary is conducting, the voltage on the secondary is reflected to the primary side of the transformer by the turns ratio. This reflected voltage V_{OR} adds to the input DC voltage at the *TOPSwitch* drain node. Worst case voltage at the drain occurs at high line when the DC input voltage is at its maximum value. The maximum DC input voltage can be calculated as:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX}$$

In addition to V_{MAX}+V_{OR} the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding (see Figures 8 and 9). To keep this voltage spike from exceeding the rated minimum drain breakdown voltage BV_{DSS}, a clamp circuit is needed across the primary winding. A Zener clamp as shown in Figure 1 is highly recommended over the usual RC clamp as it is much more effective in clamping the leakage energy during start up transients. The nominal value of Zener clamp voltage V_{CLO} needs to be 50% (determined empirically) greater than the reflected voltage so that the Zener clamps only the leakage energy and does not impede the switch-over of current from the primary to the secondary. Experimental measurements show that this voltage margin is needed for the secondary current to be quickly established through the leakage inductance. Lower clamp voltage should not be used, because part of the stored energy in the core would be delivered to the Zener, dramatically increasing Zener dissipation.

The nominal clamp Zener voltage V_{CLO} is usually specified at low current values and at room temperature. High voltage Zeners have a strong positive temperature coefficient and are quite resistive. Consequently, the clamp voltage at high current and high temperature V_{CLM} can be much higher. Experimental data has shown that the V_{CLM} can be as high as 40% above the specified V_{CLO}

$$V_{CLM} = 1.4 \times V_{CLO}$$

This needs to be taken into consideration when choosing a clamp Zener. In addition, it is important to allow an additional 20V for the spike due to the forward recovery time of the blocking diode in series with the clamp Zener. With all those factors considered, the maximum voltage that the *TOPSwitch* drain may experience is:

$$V_{DRAIN} = V_{MAX} + (1.4 \times 1.5 \times V_{OR}) + 20V$$

To minimize power supply cost, it is important to maximize the V_{OR} consistent with the *TOPSwitch* breakdown voltage rating after taking into account all of the above effects. As will be seen

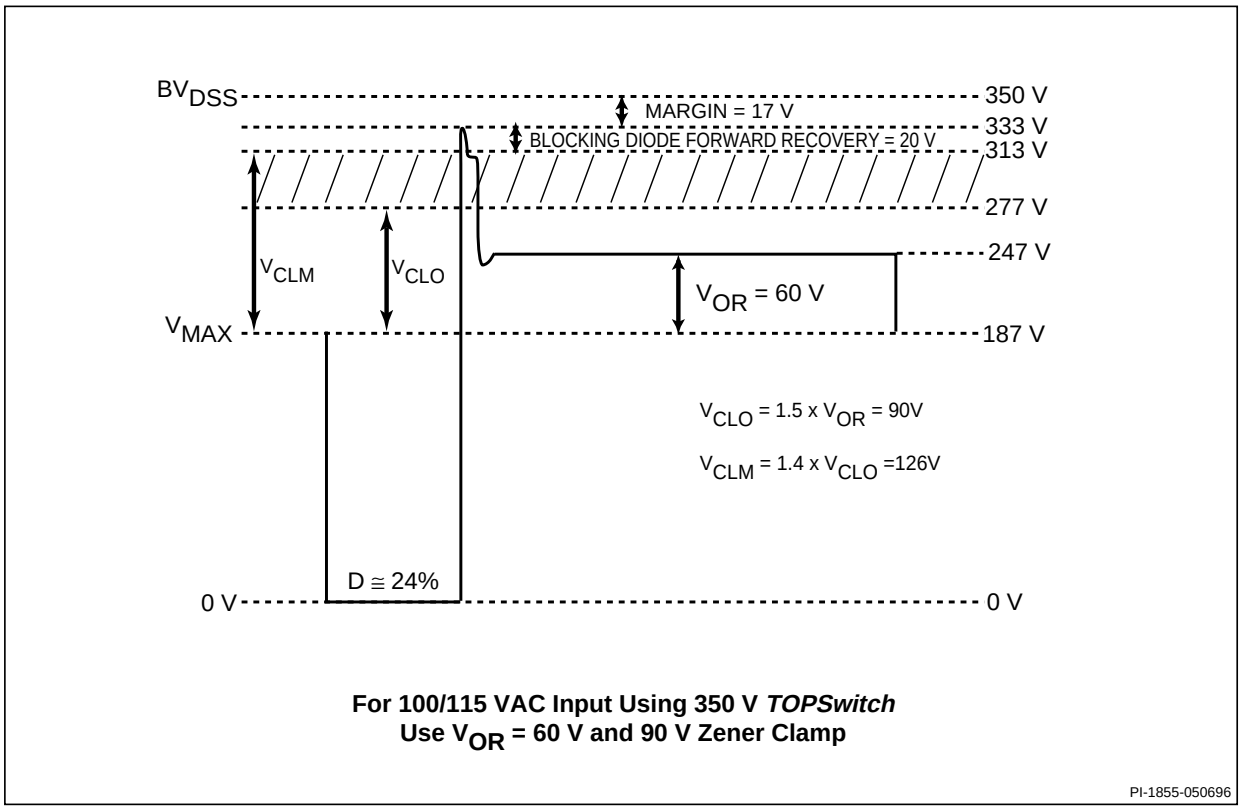

Figure 8. Reflected Voltage (V_{OR}) and Clamp Zener Voltage (V_{CLO}) - 100/115 VAC Input.

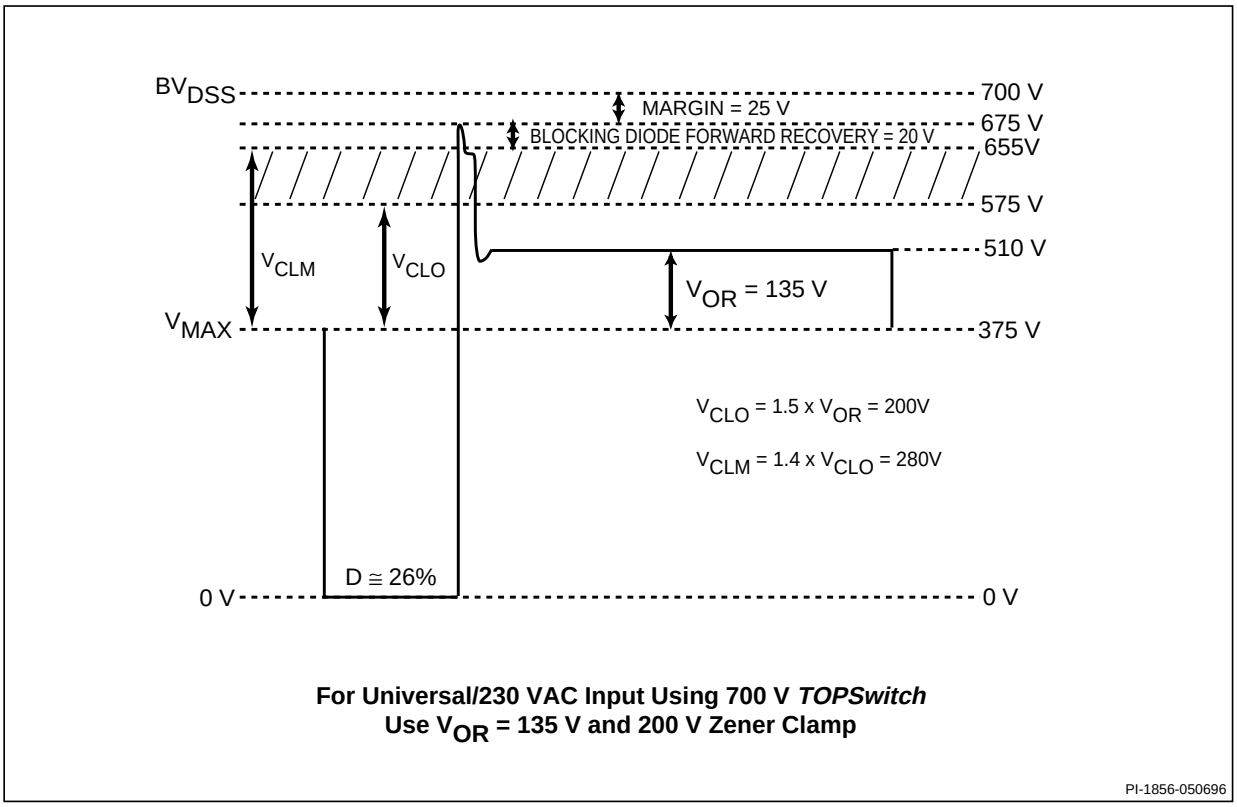

Figure 9. Reflected Voltage (V_{OR}) and Clamp Zener Voltage (V_{CLO}) - Universal/230 VAC Input.

later, a higher V_{OR} will result in a larger D_{MAX} which reduces *TOPSwitch* operating current for the same output power. If D_{MAX} comes close to the maximum allowable duty cycle of the *TOPSwitch* (64%) then V_{OR} should not be increased any further.

For a 100/115 VAC power supply the V_{ACMAX} based on 115 VAC would be 132 VAC which corresponds to:

$$V_{MAX} = \sqrt{2} \times 132 = 187V$$

As can be seen in Figure 8, going through the above exercise for a V_{MAX} of 187V using a 350V *TOPSwitch* results in a standard clamp Zener voltage of 90V and V_{OR} of 60V and a margin of 17V. Likewise in 230VAC or Universal application, a V_{ACMAX} of 265VAC corresponds to a V_{MAX} of 375V. At this value of V_{MAX}, a 700V *TOPSwitch* will allow for a standard Zener value of 200V with corresponding V_{OR} of 135V leaving a margin of 25V (see Figure 9). If these margins seem too small, it is important to remember that this analysis uses all worst case values added together and typical margins will be much greater. Also, *TOPSwitch* breakdown voltage increases at high temperature, providing additional margin.

Step 5. Determine maximum duty cycle at low line D_{MAX} using V_{OR} and V_{MIN}

Once the V_{OR} and V_{MIN} are known, it is easy to calculate the D_{MAX}:

$$D_{MAX} = \frac{V_{OR}}{V_{OR} + (V_{MIN} - V_{DS})}$$

V_{DS} is the average Drain to Source voltage during *TOPSwitch* ON time. As shown in Figures 10 and 11, with V_{DS} set to zero, the value of D_{MAX} ranges from 36%/40% for single input voltage applications to 60% for the universal input application. In reality, V_{DS} should be set to approximately 10V which results in a slight increase in D_{MAX}.

Higher V_{MIN} directly increases the output power capability of a given *TOPSwitch*, while lower V_{MAX} allows larger V_{OR} and consequently larger D_{MAX}, also increasing the output power of a given *TOPSwitch*. Therefore, a narrower input voltage range always leads to either a higher output power or a lower power supply cost.

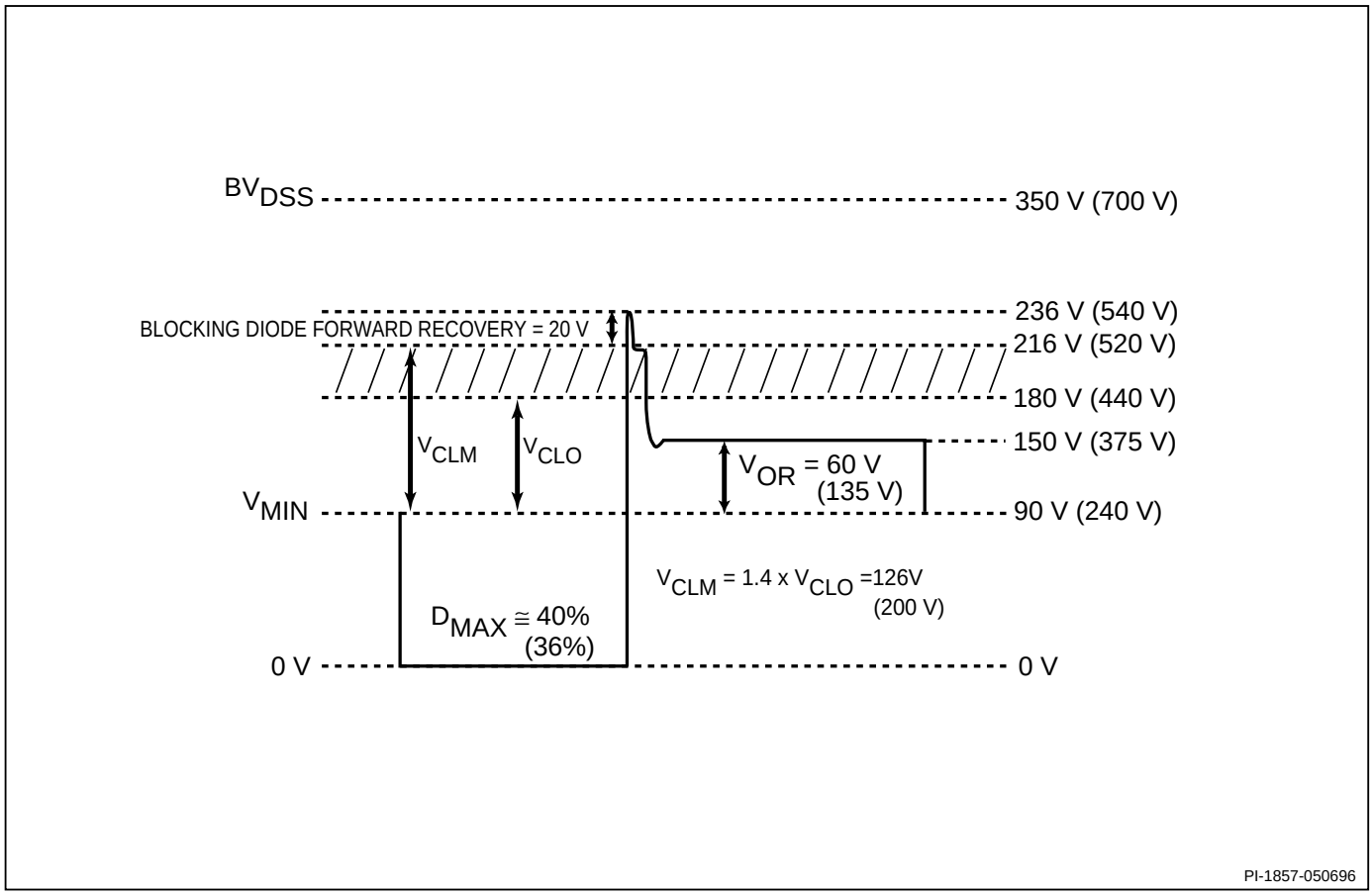

Figure 10. Determine D_{MAX} - 100/115 VAC (230 VAC) Input

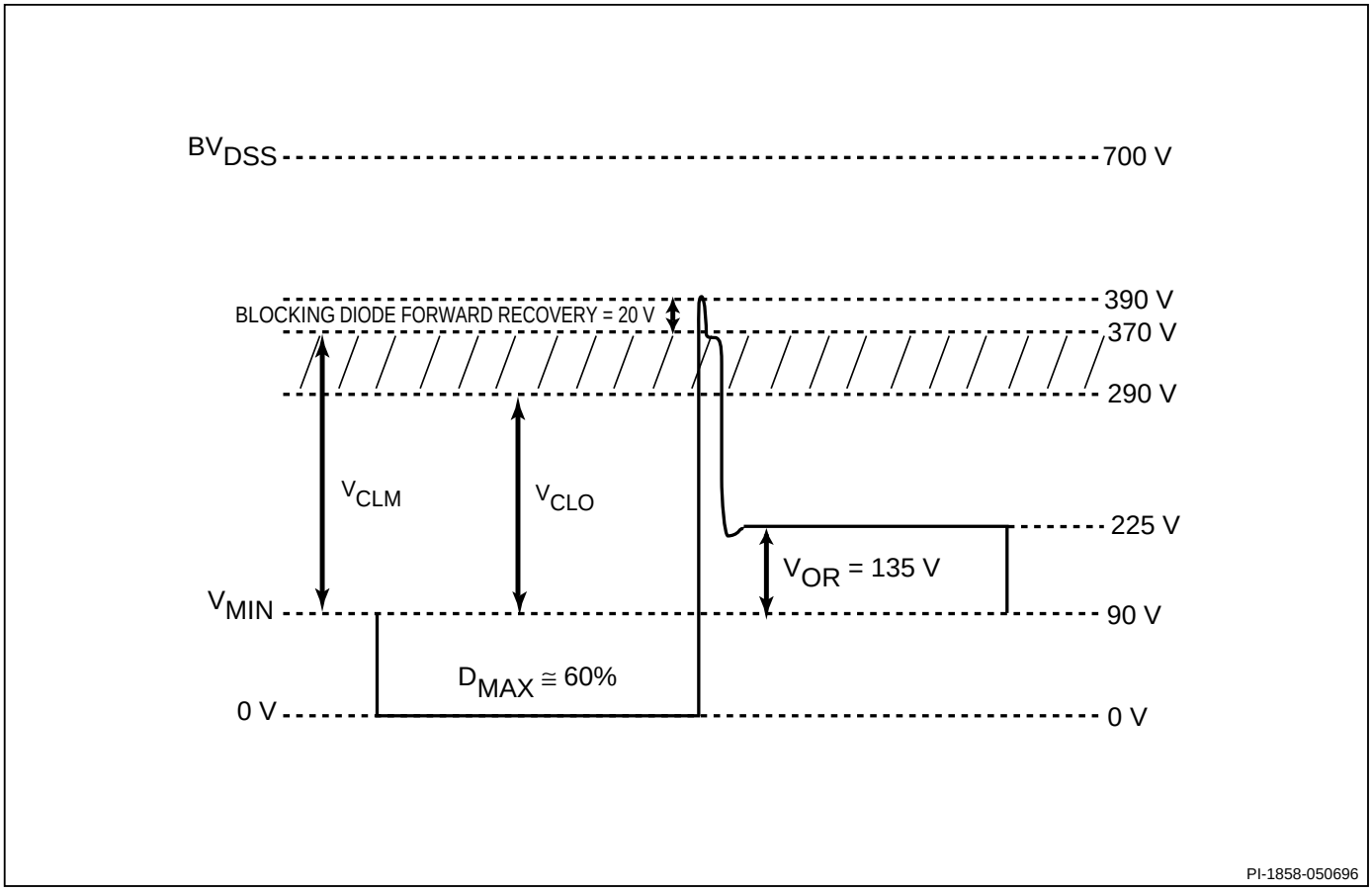

Figure 11. Determine D_{MAX} - Universal Input

Step 6. Set ripple current I_R to peak current I_P ratio K_{RP} (see Figure 12)

$$K_{RP} = \frac{I_R}{I_P}$$

- Starting with K_{RP} = 0.4 for 100/115 VAC or universal input
  0.6 for 230 VAC
  for most continuous operation
- K_{RP} may be increased to higher values for less continuous operation
- K_{RP}, by definition, can not be larger than 1.0 and may not be set smaller than above values

Many power supply design engineers prefer to use discontinuous mode (K_{RP} =1) design as the control loop is easier to stabilize. With *TOPSwitch*, because of the built-in loop compensation, it is possible to use one simple external RC network to stabilize the loop independent of operating mode. Setting K_{RP} to the values recommended above allows continuous mode operation at low input line voltage, minimizing the peak primary current for a given output power, and allowing the use of the smallest possible *TOPSwitch* for the application.

A K_{RP} of 0.6 is recommended for 230VAC (compared to 0.4 for 100/115 VAC and universal input) to accommodate a significantly taller and wider leading edge current spike caused by the discharge of the drain node capacitance at the higher voltage levels.

Step 7. Determine primary waveform parameters I_{AVG}, I_P, I_R and I_{RMS}

The average DC current I_{AVG} at low line is simply the input power divided by V_{MIN}, where the input power is equal to the output power divided by the efficiency.

$$I_{AVG} = \frac{P_O}{\eta \times V_{MIN}}$$

With K_{RP} and D_{MAX} already determined, the shape of the current waveform is known. Due to the simple geometry of the waveform, the Primary peak current I_P, ripple current I_R and RMS current I_{RMS} can be easily derived as a function of I_{AVG}:

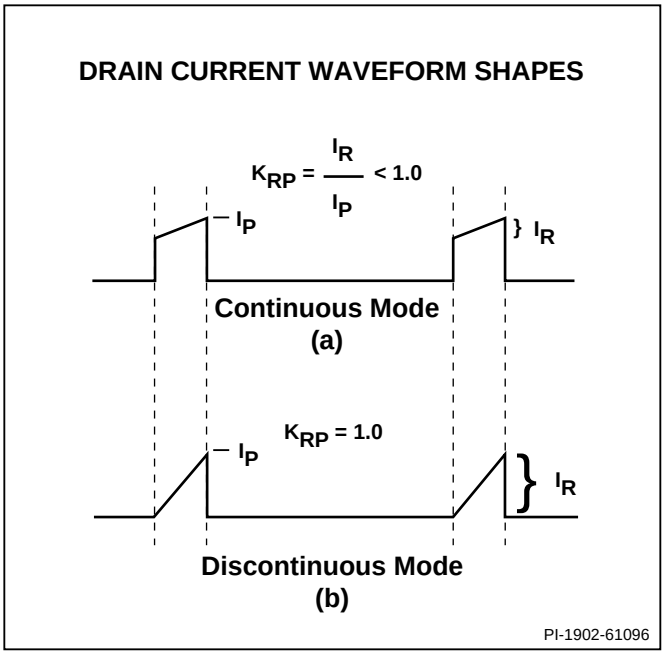

Figure 12. Primary Current Waveform.

$$I_P = \frac{I_{AVG}}{\left(1 - \frac{K_{RP}}{2}\right) \times D_{MAX}}$$

$$I_R = I_P \times K_{RP}$$

$$I_{RMS} = I_P \times \sqrt{D_{MAX} \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1\right)}$$

Step 8. Select *TOPSwitch* based on *TOPSwitch* data sheet minimum I_{LIMIT} specification and required I_P (from Step 7) such that:

$$0.9 \times \text{minimum } I_{LIMIT} \geq I_P$$

The minimum value of current limit I_{LIMIT} in *TOPSwitch* data sheet is specified at room temperature. To accommodate the slight reduction of this parameter at high temperature, the room temperature limit should be derated by 10%. This can be accomplished by dividing the I_p by 0.9 and comparing this value to the minimum I_{LIMIT} in the datasheet. The smallest *TOPSwitch* that has an I_{LIMIT} higher than this value should be selected as the first choice for the lowest cost.

Step 9 to Step 10. Check thermal limitation - Use bigger *TOPSwitch* if necessary to reduce power loss

- Calculate *TOPSwitch* conduction loss at low line:

$$P_{IR} = I_{RMS}^2 \times R_{DS(ON)}(100°C)$$

- Calculate *TOPSwitch* switching loss at low line:

$$P_{CXT} \cong \frac{1}{2} \times C_{XT} \times (V_{MAX} + V_{OR})^2 \times f_S$$

  where C_{XT} is the external capacitance at the drain node.

- Calculate junction temperature Tj of *TOPSwitch* as a function of total loss

$$T_J = 25°C + (P_{IR} + P_{CXT}) \times \theta_{JA}$$

- If Tj > 100°C, choose bigger *TOPSwitch*.

- For non-critical applications, refer to AN-14 Table 2 for *TOPSwitch* recommendations with practical heatsinking.

TOPSwitch thermal environment can vary significantly from application to application. Fully enclosed lap top adapters with no ventilation pose significant limitations on the power that can be dissipated inside the box without exceeding acceptable surface temperatures on the outside of the box. Heat sinks in this application only help to distribute the heat across the surface of the box. The actual power capability at a given surface temperature is determined largely by the surface area of the box. In contrast, a PC power supply has a fan which provides forced air cooling. Here a larger heat sink could be the answer to higher power dissapation.

It is therefore important to first estimate the losses in the *TOPSwitch* to see whether it is acceptable in a given application. The conduction losses (P_{IR}) at low line tend to be the dominant loss factor and can be calculated using the I_{RMS} and the $R_{DS(ON)}$ at 100°C from the output characteristic curve in the *TOPSwitch* data sheet. If the losses are unacceptable, a larger *TOPSwitch* with a lower $R_{DS(ON)}$ could be chosen to lower the power dissipation.

Switching losses at low line due to internal drain capacitance are negligible and can be ignored. If significant external capacitance C_{XT} is present, the switching losses (P_{CXT}) should also be estimated. Even though low line is usually the worst case for *TOPSwitch* losses, it is prudent to verify this by calculating the conduction and switching losses at high line, especially if there is significant external capacitance on the drain.

Once the worst case loss in the *TOPSwitch* is known, the maximum die temperature at worst case ambient (internal ambient should be used for enclosed supplies) can be estimated using the thermal impedance from die to tab/heat sink of the

package, $Ø_{JC}$ (specified in the *TOPSwitch* datasheet), and from heat sink to ambient, $Ø_{CA}$ (usually specified in the heat sink data sheet). If a package without a heatsink tab is used, such as an 8 pin DIP, then a typical die to ambient thermal impedance, $Ø_{JA}$, for a board mounted part can be found in the data sheet for these calculations. It is recommended that the die temperature be kept below 100°C under all conditions.

Step 11. Check minimum I_{LIMIT} of the selected *TOPSwitch* against required I_P. Increase K_{RP}, if possible, for least continuous operation.

Using continuous mode operation at low line decreases the peak current required for a given output power, allowing the use of a smaller *TOPSwitch*. However, if so desired, a trade-off between *TOPSwitch* and core size can be accomplished by increasing the K_{RP} value. Larger K_{RP} allows the use of a smaller core at the price of a larger *TOPSwitch*, as larger K_{RP} implies less continuous operation and lower inductance L_P, but higher peak current I_P. This is very important when the best suited (smallest possible) *TOPSwitch* that can be chosen for a design still ends up with significant extra current capability. It is then best to trade this extra current capability for a reduced core size by using a higher K_{RP}. In addition to affecting the size of the transformer core, K_{RP} also influences supply efficiency. Larger K_{RP} results in higher primary RMS current I_{RMS} and higher *TOPSwitch* conduction loss while lower K_{RP} results in lower I_{RMS} and lower *TOPSwitch* loss. For applications with tight physical size/weight limitation and/or efficiency requirements, an intermediate K_{RP} value can offer the optimum solution between cost and performance.

Although this design method is designed to use the highest possible K_{RP} once *TOPSwitch* is first chosen, the flexibility is certainly available for other design options. Experienced engineers should make their own judgment on K_{RP} value based on the specific requirements of their application.

Step 12. Determine primary inductance L_P

Because the energy transferred from primary to secondary each switching cycle is simply the difference between $1/2 \times L_p \times I_p^2$ and $1/2 \times L_p \times (I_p - I_R)^2$. The primary inductance L_p can be expressed as a function of I_P, K_{RP}, f_S, P_O, η and Z:

$$L_P = \frac{10^6 \times P_O}{I_P^2 \times K_{RP} \times \left(1 - \frac{K_{RP}}{2}\right) \times f_S} \times \frac{Z \times (1-\eta) + \eta}{\eta}$$

η is the efficiency and Z is the loss allocation factor. If Z=1, all losses are on the secondary side. If Z = 0, all losses are on the primary side. Z is simply the ratio of secondary loss to total loss. If no better reference information is available, Z should be set to 0.5.

Step 13. Chose core and bobbin as a function of P_O based on AN-18, Appendix A, Table 2 and determine A_e, L_e, A_L and BW from core and bobbin catalog

AN-18 Appendix A provides a table of recommended core types for various power ranges. Notice that there are two transformer construction types shown in the table. For single output designs, a triple insulated secondary simplifies transformer construction and allows the use of the smallest size core and bobbin for a given output power. Margin winding, which is suitable for both single and multiple output secondaries, will require wider bobbins and therefore, longer/taller cores. If there is no specific form factor requirement, it is best to start with the smallest EE type core for the power level. EE cores are usually the least expensive type. The two digit number following the core type indicates the core size in mm. For 100KHz operation, the selection of core material is not very critical. TDK PC40 material is a good first choice. Other ferrite materials with similar characteristics are available from many manufacturers. Lower frequency core materials such as Philips 3C85 and its equivalents will also work at 100 KHz, and could be used if there is a cost advantage.

Once a core has been selected from the catalog, a suitable bobbin can be easily identified.

Manufacturer specified core parameters A_e, L_e, A_L and bobbin parameter BW are usually found in the same catalog.

Step 14. Set number of primary layers L and number of secondary turns N_S

(see Step 16 to 22)

Step 15. Calculate number of primary turns N_P and number of bias turns N_B

(see Step 16 to 22)

Step 16 to Step 22. Check B_M, CMA and L_g. Iterate if necessary by changing L, N_S, core/bobbin until within specified range

In addition to the selection of core and bobbin, a total of nine parameters must be specified in the construction of a transformer: primary inductance Lp, core gap length L_g, number of turns for primary N_P, secondary N_S and bias N_B, wire outside diameter for primary OD and secondary OD_S, bare conductor diameter for primary DIA and secondary DIA_S. Because the bias winding carries very little current (typically less than 10 mA), the wire size of the bias winding is never a problem.

Except for L_P, the above parameters are all interdependent. A good starting point is to pick a number for the secondary turns. Using 1 turn/volt for 100/115 VAC and 0.6 turn/volt for 230 VAC

or universal inputs is a good assumption. As an example, for a 115VAC input and an output voltage V_O of 15V plus the rectifier forward drop V_D of 0.7V, a 16 turn secondary would be used as the initial value. The primary number of turns N_P is related to the secondary number of turns N_S by the ratio between V_{OR} and $V_O + V_D$

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

where V_{OR} is the reflected output voltage, V_O is the output voltage and V_D is the output rectifier forward voltage drop.

Similarly, the number of bias winding turns N_B can be derived from

$$N_B = N_S \times \frac{V_B + V_{DB}}{V_O + V_D}$$

where V_B is the bias voltage and V_{DB} is the bias rectifier forward voltage drop.

From the core/bobbin size, it is possible to determine the outside diameter of the primary wire OD in mm that is required to accommodate the primary turns in one or two full layers allowing for margins as appropriate.

$$OD = \frac{BW_E}{N_P}$$

BW_E is the effective bobbin width, which takes into account physical bobbin width BW, margins M (all in mm), and the number of winding layers L:

$$BW_E = L \times [BW - (2 \times M)]$$

The closest standard magnet wire gauge that is less than or equal to this diameter can be selected. Determine the bare conductor diameter DIA of this wire gauge using information from a wire table. The next step is to find out if this conductor size is sufficient for the maximum I_{RMS}. The current capacity for magnet wire is specified in terms of "Circular mils per Amp" or CMA, which is the inverse of current density:

$$CMA = \frac{1.27 \times DIA^2 \times \frac{\pi}{4}}{I_{RMS}} \times \left(\frac{1000}{25.4}\right)^2$$

If the CMA is less than 200, a larger gauge wire is needed to handle the current. This could be accommodated by adding a second layer if there is only one existing layer and/or by using a larger core/bobbin and/or a smaller N_P. On the other hand, a CMA greater than 500 would indicate that a smaller core/bobbin and/or a larger N_P could be used.

Note that in the AN-17 spreadsheet, DIA is actually derived from OD using an empirical equation. A practical wire size, AWG (American Wire Gauge), is determined according to DIA (see AN-18 Appendix A, Table 2 for wire size information). CMA is then calculated from AWG.

Another critical parameter that must be checked is the maximum flux density in the core (B_M).

$$B_M = \frac{100 \times I_P \times L_P}{N_P \times A_e}$$

A_e is the effective cross sectional area of the core.

If B_M is greater than 3000 Gauss, either the core cross sectional area (core size) or N_P must be increased to bring it within the 2000 to 3000 range. On the other hand, if B_M is less than 2000 Gauss, a smaller core or fewer turns on the primary can be used.

In addition to B_M, the core gap length L_g required to generate inductance L_P with number of primary turns N_P must also be checked:

$$L_g = 40 \times \pi \times A_e \times \left(\frac{N_P^2}{1000 \times L_P} - \frac{1}{A_L}\right)$$

The core cross sectional area A_e and ungapped effective inductance A_L can be found from the data sheets for the core. L_g is usually incorporated as an air gap ground into the center leg of the core and needs to be at least 51 µm or (2 mils) for manufacturability. If L_g is less than 51 µm, once again the core size or N_P must be increased.

One other parameter always required by transformer manufacturer is the gapped core effective inductance, A_{LG}, which can be determined only after N_P is fixed:

$$A_{LG} = 1000 \times \frac{L_P}{N_P^2}$$

As can be seen, the transformer design is a highly iterative process in itself. When N_P is changed, N_S and N_B will change according to ratios already established. Similarly, any change in core size requires a recalculation of CMA, B_M and L_g to make sure that they are within the specified limits.

Step 23. Determine secondary parameters I_{SP}, I_{SRMS}, I_{RIPPLE}, DIA_S, OD_S

The secondary peak current I_{SP} can be derived from the primary peak current I_P and the turns ratio between primary and secondary N_P/N_S

$$I_{SP} = I_P \times \frac{N_P}{N_S}$$

The K_{RP} of the secondary is always identical to that of the primary, since it is only a reflected version of the primary current with duty cycle (1-D). Therefore, the secondary RMS current I_{SRMS} can be expressed in a manner similar to the primary RMS current, only with D_{MAX} replaced by $(1\text{-}D_{MAX})$.

$$I_{SRMS} = I_{SP} \times \sqrt{(1 - D_{MAX}) \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1 \right)}$$

I_{RIPPLE} is the RMS ripple current of the output capacitor. Because of current conservation, it is found that:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

I_O is the power supply output current which can be calculated, if not already specified, as

$$I_O = \frac{P_O}{V_O}$$

With the secondary RMS current I_{SRMS} available, the minimum secondary wire diameter DIA_S (in mm), can be calculated as follows:

$$DIA_S = \sqrt{\frac{4 \times CMA \times I_{SRMS}}{1.27 \times \pi}} \times \frac{25.4}{1000}$$

Note that in the AN-17 spreadsheet, a practical wire size, AWG_S, is derived from primary current capacity CMA and secondary RMS current I_{SRMS} using an empirical equation. DIA_S is then determined from AWG_S.

If the required secondary wire diameter turns out to be larger than that of the 26 AWG wire which corresponds to twice the skin depth at 100 KHz, a parallel configuration of windings using a gauge equal to or smaller than 26 AWG should be used to provide the same effective cross sectional area. The parallel windings must have identical number of turns equal to N_S. For example, if the equation above indicates a 23 AWG wire, a winding consisting of N_S turns of two parallel strands of 26 AWG will be a good choice.

Note that if triple insulated wire is to be used for secondary, the insulated wire diameter is actually larger than DIA_S by twice the thickness of the insulator. Therefore, the maximum outside diameter OD_S (in mm) must be calculated:

$$OD_S = \frac{BW - (2 \times M)}{N_S}$$

A triple insulated wire should be specified with a conductor diameter equal to or greater than DIA_S and an insulated outside diameter equal to or less than OD_S.

Step 24. Determine maximum peak inverse voltages PIV_S, PIV_B for secondary and bias windings.

The peak inverse voltage across the secondary rectifier diode is given by:

$$PIV_S = V_O + \left(V_{MAX} \times \frac{N_S}{N_P} \right)$$

Similarly, the peak inverse voltage across the bias rectifier diode is given by:

$$PIV_B = V_B + \left(V_{MAX} \times \frac{N_B}{N_P} \right)$$

Step 25. Select clamp Zener and blocking diode for primary clamping based on input voltage and V_{CLO}

(see Step 4)

Step 26. Select output rectifier

The peak inverse voltage across the secondary diode PIV_S is calculated in Step 24. The diodes should be chosen with a reverse voltage rating V_R equal to or greater than 1.25 X PIV_S to keep the PIV_S at no more than 80% of the diode V_R rating.

The rule of thumb on the diode current rating is to choose one with rated DC current of at least three times the maximum output DC current.

Schottky diodes are recommended for V_R less than 45V which would correspond to low output voltages such as 5V or 3.3V. For V_R requirements that are higher than 45V, ultra fast recovery PN diodes should be used for the lowest cost. (See Table 8 for recommended diodes.)

Step 27. Select Output capacitor

ESR is the most important parameter for output filter capacitor selection. Capacitor ESR directly determines the output ripple voltage of the power supply and the ripple current rating of the capacitor while the actual capacitance value only affects control loop bandwidth. Below 35V, ESR is mainly determined by capacitor case size. Consider two Nichicon PL series capacitors: 1500µF/6.3V and 390µF/35V. Both capacitors have a case size of 10 mm diameter and 25 mm length, and both have the same ESR of 55 mΩ. To keep control loop bandwidth high, the smaller capacitance, higher voltage rating capacitor is preferred.

Ripple current is typically specified at 105°C ambient which is much higher than the ambient temperature required in most applications. Therefore, it is possible to operate the capacitor at higher ripple currents determined by a multiplier factor from the capacitor data sheet.

Actual ripple current of the output capacitor can be calculated as follows:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

where I_{SRMS} is the secondary winding RMS current and I_O is the DC output current.

Step 28 to Step 29. Select Output post filter L, C

If the measured switching ripple voltage at the output capacitor is higher than the required specification, an LC post filter consisting of a 2.2 to 4.7µH inductor or ferrite bead (only for power levels below 5W) with a 120 uF/35V, low ESR electrolytic capacitor is recommended. This will provide a lower cost solution compared to increasing the capacitance value and/or lowering the ESR of the main output filter capacitor.

The output post filter, to a first order, is independent of output power except that the DC voltage drop across the inductor may be a concern at high currents. Inductors with larger gauge wire and higher current rating solve this problem.

Step 30. Select bias rectifier

Bias rectifier selection is similar to output rectifier selection with the exception that since the bias winding carries very little current (typically less than 10 mA), the considerations for current capability and very fast recovery no longer apply.

Step 31. Select bias capacitor

Because of the low voltage and the minimal power required at the bias output, a 0.1 uF, 50V ceramic capacitor always meets the requirement.

Step 32. Select Control pin capacitor and series resistor

A 47 µF, 10V low cost standard grade electrolytic capacitor across the Control pin and Source pin of the *TOPSwitch* takes care of loop compensation for all types of feedback configurations. Low ESR capacitors should not be used for this purpose, as the ESR resistance of the standard grade capacitor (2 Ω typical) improves the loop stability by introducing a zero. In fact, a 6.2Ω resistor in series with this capacitor is recommended to improve phase margin in designs that either have excessive gain in the secondary (such as the TL431 circuit shown in Figure 6), or a K_{RP} value of less than one (continuous mode).

Step 33. Select feedback circuit components

- Primary feedback: Refer to RD1
- Opto/Zener feedback: Refer to ST202A
- Opto/TL431: Refer to ST204A
- Select opto-coupler with CTR between 50% and 200% (Refer to AN-14, Table 3)

Step 34. Select bridge rectifier based on input voltage V_{ACMAX} and input RMS current I_{ACRMS}

Maximum operating current for the input bridge rectifier occurs at low line:

$$I_{ACRMS} = \frac{P_O}{\eta \times V_{ACMIN} \times PF}$$

PF is the power factor of the power supply. Typically, for a power supply with a capacitor input filter, PF is between 0.5 and 0.7. Use 0.5 if there is no better reference data available.

Select the bridge rectifier such that:

- $I_D \geq 2 \times I_{ACRMS}$, where I_D is the rated RMS current of the bridge rectifier
- $V_R \geq 1.25 \times 1.414 \times V_{ACMAX}$; where V_R is the rated reverse voltage of the rectifier diode

Step 35. Design complete

Following the step-by-step procedure completes the design of a basic *TOPSwitch* flyback converter. Once built, the power supply should be fully functional and capable of delivering maximum rated output power at minimum input line voltage, while meeting all specifications. Minor adjustments may be necessary to center the output voltage.

Issues Beyond the Design Method

Issues outside the basic converter requirements are beyond the scope of this application note. However, design guidelines for various issues are available in the following documentation:

- Constant current/power output : DN-14
- PC board layout : AN-14
- Transformer design : AN-17
- Transformer construction : AN-18
- Efficiency : AN-19
- EMI and safety : AN-15
- Transient : AN-20

Application specific requirements such as constant current and/or constant power outputs (DN-14), input under voltage protection, soft start etc. (refer to AN-14) are usually implemented by adding minimal circuitry to the basic converter.

General design guidelines for EMI, safety and input transient are provided in AN-15 and AN-20 respectively. However, the optimum solution for any particular design can only be found through experimentation.

Transformer construction techniques are very critical in the successful development of a *TOPSwitch* flyback. AN-18 provides practical guidelines that should be followed carefully to minimize parasitics such as leakage inductance, inter-winding capacitance etc.

Appendix A
TOPSwitch Flyback Fundamentals

This appendix explains the operation of a flyback power supply using the *TOPSwitch* power integrated circuit. *TOPSwitch* is a monolithic device combining a high voltage power MOSFET switch with all the analog and digital control circuitry required to implement isolated, regulated, and protected switching power supplies. Designing the power supply is greatly simplified because few external components are required. The high switching frequency of 100 KHz reduces the size of the power supply by allowing the use of smaller energy storage components. The *TOPSwitch* was designed for use in isolated power supplies or DC to DC converters. Power levels up to 50 Watts can be delivered from AC voltages of 85 to 265 VAC, or 100W with a 195 to 265 VAC input range. Operation from lower input voltages is also possible with reduced levels of output power.

The flyback power supply is described in detail. Ideal and non-ideal circuit operation is explained. The difference between the discontinuous and continuous mode of operation is discussed. The benefits of high frequency operation are presented. Other types of power supplies using both linear and switching techniques are examined and compared with the flyback topology.

The Flyback Power Supply

The flyback topology, shown in Figure 1, is recommended for off-line, isolated, power supply applications. The flyback supply has a low parts count, wide input voltage range, inherent feedback voltage sensing, single or multiple output voltage capability, output voltages that can be higher or lower than the input voltage, and ability to provide both positive and negative voltages.

Almost all off-line switching power supplies require isolation between primary and secondary components to satisfy the requirements of domestic and international safety regulations. This isolation, along with any necessary voltage transformation, requires a power transformer. Most switching power supplies also need an inductor as the energy storage component and also as part of the low pass filter required to transform the pulse width modulated switching waveform into a DC output. The flyback topology is attractive for low power isolated switching power supplies because the transformer is combined with the inductor in a single magnetic component providing energy storage, isolation, and voltage transformation. As compared to other topologies such as the forward converter, the flyback has the fewest magnetic components and the lowest parts count, resulting in the lowest cost. The flyback topology retains these advantages at power levels up to 100 watts, or output currents up to 10 amperes. Component stress levels above 100 watts or 10 amperes output current require the use of more expensive components, allowing other topologies to become more cost effective.

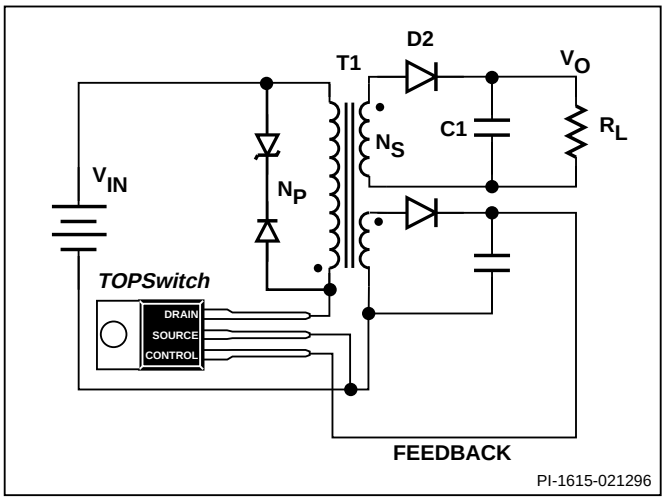

Figure 1. Basic Flyback Converter Circuit.

Another important advantage of the flyback topology is that a feedback voltage proportional to the output voltage can be obtained directly by adding a “feedback” winding to the power transformer. This means that secondary side regulation can be accomplished on the primary side of the power supply without using an optocoupler or similar isolation device between the primary and secondary circuitry. Single or multiple, higher or lower, positive or negative output voltages are primarily a function of the construction of the power transformer.

Comparison to Other Techniques

Alternatives to flyback power supplies for low power applications include linear supplies and other switching topologies such as the buck converter and the forward converter. These are briefly examined below. Additional information can be found in some of the references listed at the end of this appendix.

Linear Power Supplies

The linear power supply is characterized by the use of an AC line frequency (50-60 Hz) transformer, rectifier, filter, and linear regulator as shown in Figure 2. This type of power supply is inexpensive and reliable but suffers from the following disadvantages:

- Largest size
- Highest weight
- Poorest efficiency
- Narrow input voltage range

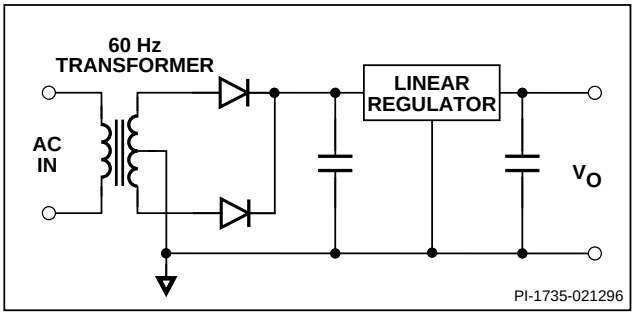

Figure 2. Linear Regulator Circuit.

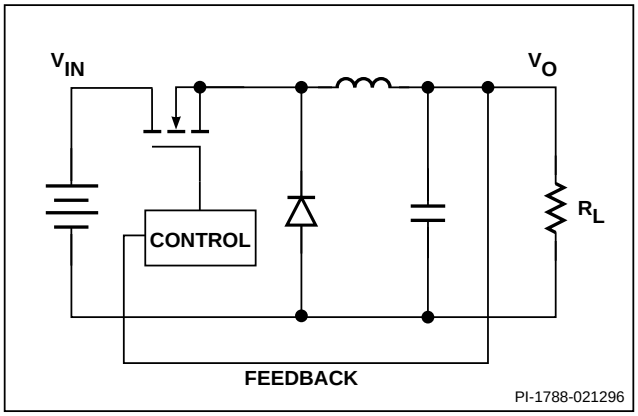

Figure 3. Buck Converter Circuit.

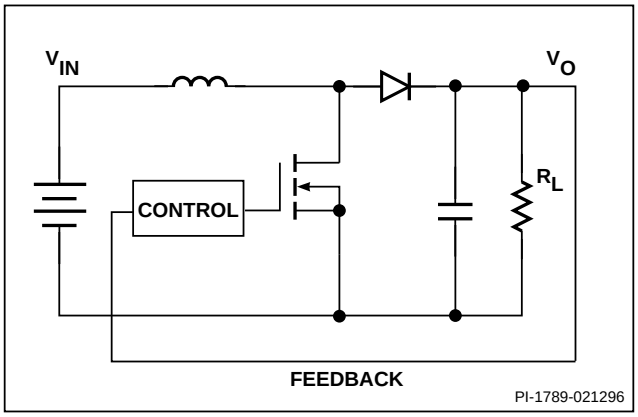

Figure 4. Boost Converter Circuit.

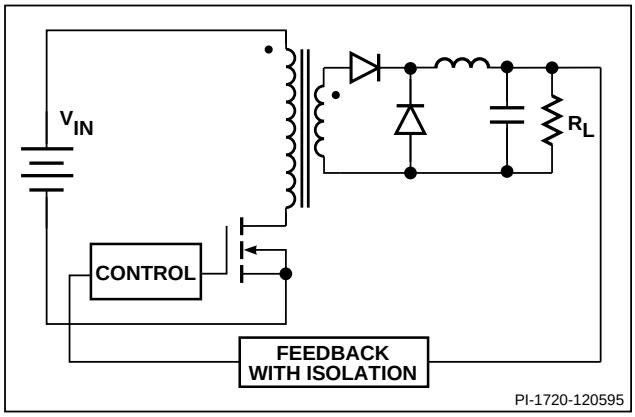

Figure 5. Forward Converter Circuit.

Switching Power Supplies

There are many different switching power supply topologies available. The buck, boost, and forward converters are described below. Multiswitch and resonant converters are also briefly discussed.

Buck Converter - The buck converter, shown in Figure 3, is useful for stepping down from a higher voltage to a lower voltage. The key points are:

- Not isolated
- High side switch requires level shift or bootstrap circuit to drive
- Limited to approximate 10:1 conversion range by duty cycle requirements
- Provides only down converted, positive output voltages

Boost Converter - The boost converter, shown in Figure 4, is useful for stepping up from a lower voltage to a higher voltage. The key points are:

- Not isolated
- Limited to approximate 10:1 conversion range by duty cycle requirements
- Provides only up converted, positive output voltages

Forward Converter - The forward converter, shown in Figure 5, is an isolated version of the Buck. Single or multiple, positive or negative, higher or lower output voltages are available by transformer design. This topology can be useful for output power of 100 W to 300 W. The key points are:

- Inductor required for each output voltage
- Extra diode required for each output voltage
- Additional isolated feedback circuit required

Multiple Switch Converters - Multiple switch converter topologies include the push-pull, half bridge, full bridge, two transistor flyback, and two transistor forward converters. All these circuits require at least one additional power switch and are much more complex and costly. They are used to implement power supplies ranging from 200 watts to several kilowatts and are inappropriate for low power, low cost designs.

Resonant and Quasi-Resonant Converters - Resonant converters are switching power supplies that use resonant tank circuits to process power with sinusoidal waveforms rather than the pulse width modulated quasi-square waves employed by conventional switching power supplies. Quasi resonant power supplies are switching power supplies that use resonant circuits to smooth the turn on and turn off edges in the switching waveform. In general, resonant and quasi-resonant converters are used at frequencies considerably higher than 100 KHz, and require more components than the traditional quasi-square wave

switching power supply. Peak voltage or current stress levels are higher than quasi square wave power converters, depending on whether a zero-voltage switching or a zero-current switching topology is used. The most effective resonant converters use both high side and low side switches, adding to circuit complexity. Resonant converters are not cost effective at low output power levels.

Flyback Theory

Basic Flyback Operation

A basic flyback power supply circuit utilizing *TOPSwitch* is shown in Figure 1. Transformer T1 is used both for energy storage, output isolation, and output voltage transformation. When the *TOPSwitch* is on, secondary diode D2 is reverse biased, and current ramps up in the transformer primary winding according to the equation

$$I_{PRI} = I_I + \frac{(V_{IN} - V_{DS(ON)}) \times t_{ON}}{L_P} \qquad (1)$$

I_{PRI} is the primary current in amperes, I_I is the initial value of the primary current in amperes, V_{IN} is the DC input voltage after the bridge, $V_{DS(ON)}$ is the drain to source voltage drop across the *TOPSwitch* output MOSFET, t_{ON} is the on time of the *TOPSwitch*, and L_P is the transformer primary inductance in Henries. Since the transformer is isolated from the output load circuit by the reverse biased D2, energy is supplied to R_L from the output capacitor C1 during the *TOPSwitch* on time.

When the *TOPSwitch* turns off, the magnetic flux in the transformer core starts to decay, and the polarity of the secondary winding is reversed. D2 turns on, and the energy stored in the transformer during the on time of the *TOPSwitch* is discharged into the load circuit, supplying current to the load R_L and replenishing the charge depleted from C1 during the on time. The initial value of the secondary current at the instant the *TOPSwitch* turns off will be equal to I_P x N_S/N_P, where I_P is the peak value of I_{PRI} at the end of *TOPSwitch* on time and N_P is the number of primary turns and N_S is the number of secondary turns. The secondary current decays from its initial value according to Equation (2).

$$I_{SEC} = \frac{I_P \times N_P}{N_S} - \frac{(V_O + V_{D2}) \times t_{OFF} \times N_P^2}{N_S^2 \times L_P}$$
$$(I_{SEC} \geq 0) \qquad (2)$$

V_O is the output voltage of the supply, V_{D2} is the forward voltage drop of D2, and t_{OFF} is the *TOPSwitch* off time. If the secondary current decays to zero during the off time of the primary switch, the output current is then supplied by the output capacitor C1.

There are two distinct modes of flyback supply operation, depending on the value of I_{SEC} at the end of the *TOPSwitch* off time. If I_{SEC} decays to zero at or before the end of the *TOPSwitch* off time, the supply is running in the discontinuous mode. If I_{SEC} is greater than zero at the end of the off time, the supply is running in the continuous mode of operation.

Ideal Model (Discontinuous Mode)

There are three distinct intervals of circuit operation for flyback power supplies operating in the discontinuous mode as shown in Figure 6.

The first interval (1) of operation occurs when the *TOPSwitch* is on. Current I_{PRI} ramps up linearly in the transformer primary winding, causing a magnetic field to build in the transformer

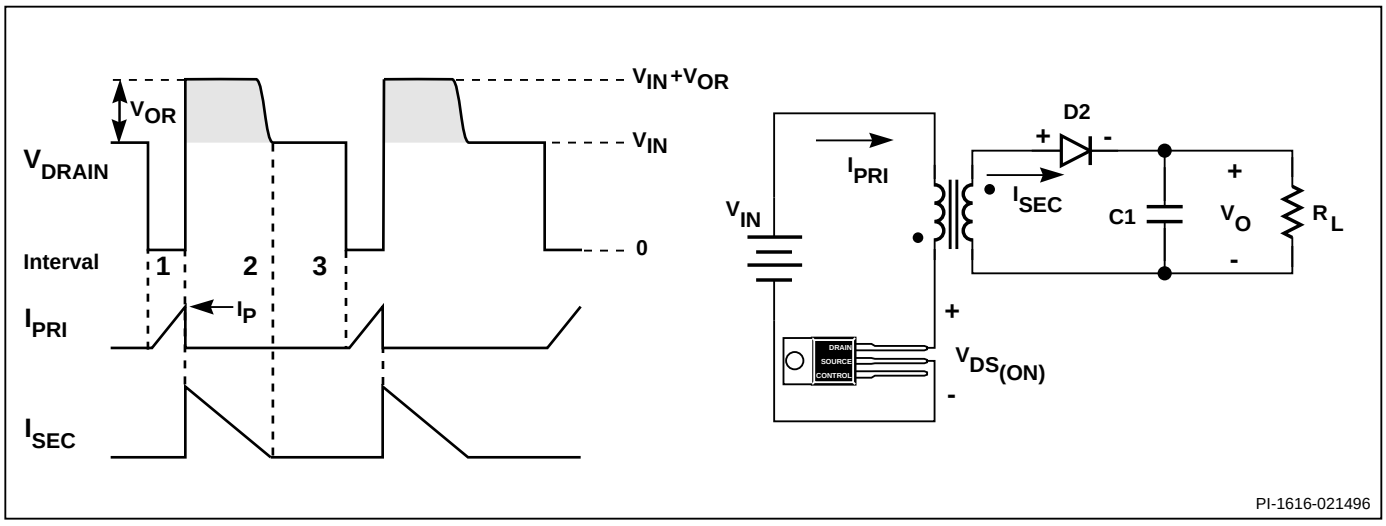

Figure 6. Ideal Flyback Converter Waveforms - Discontinuous Mode.

core. The drain to source voltage $V_{DS(ON)}$ across *TOPSwitch* is nearly zero during this interval. The output diode prevents current flow in the secondary due to the transformer dot polarity. Since the transformer secondary is isolated from the output by the reverse biased diode D2, current is supplied to the output from C1.

The second interval (2) of operation starts when *TOPSwitch* turns off. The energy stored in the magnetic field of the transformer causes the voltage across both the primary and secondary windings to reverse polarity. In an ideal circuit the primary current I_{PRI} instantly stops flowing while the secondary current I_{SEC} instantly starts flowing (it will be shown later how important it is to consider non-ideal behavior). The voltage across the secondary winding is equal to the sum of the output voltage and diode forward voltage. The secondary voltage is "reflected" back through the transformer turns ratio to the primary winding. Note that the drain to source voltage across the *TOPSwitch* during this interval of operation is equal to the sum of the reflected output voltage V_{OR} and the input voltage V_{IN}. This reflected voltage must be taken into account when selecting the transformer turns ratio to avoid excessive voltage stress on *TOPSwitch*. The reflected voltage can also be used to indirectly sense the output voltage of the supply from the primary side of the transformer through a bias or control winding referenced to the primary return, making primary side control of the supply possible.

The energy stored in the primary inductance of the transformer during the first interval of operation supplies current to the load circuit during the second interval of operation and replenishes the charge depleted from output capacitor C1 during the first and third intervals.

The third interval (3) of operation occurs when the magnetic field within the core has decayed to zero ($I_{SEC} = 0$). No current flows in the primary or secondary of the transformer (which defines the discontinuous mode of operation). Note that the drain to source voltage across the *TOPSwitch* has decayed to the level of the input voltage. Since the stored energy of the transformer has decayed to zero, the output load current is again supplied by output capacitor C1.

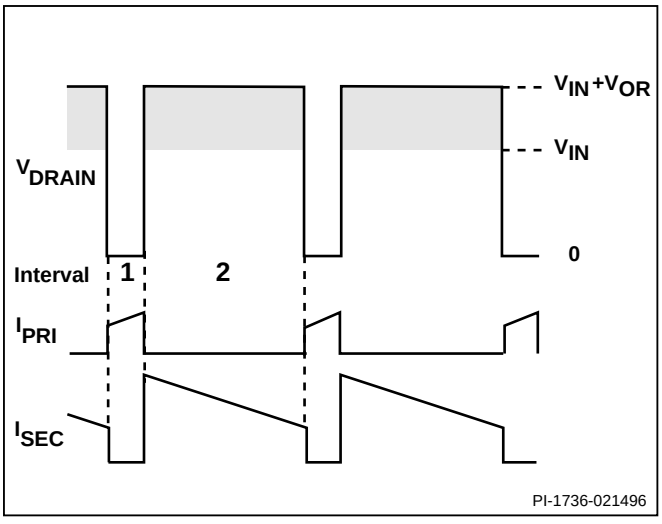

Figure 7. Ideal Flyback Converter Waveforms - Continuous Mode.

The energy delivered to the load each cycle by the transformer is given by

$$E = \frac{1}{2} \times L_P \times I_P^2 \times \eta$$

thus the output power is defined by

$$P_O = \frac{1}{2} \times L_P \times I_P^2 \times \eta \times f_S$$

where f_S is the operating frequency of the power supply, and η is the efficiency. Substituting the expression of Equation (1) for I_P (with $I_I = 0$ and $V_{DS(ON)} = 0$), and defining t_{ON} as D/f_S, where D is the duty cycle, and f_S is the *TOPSwitch* operating frequency. One obtains the expression

$$P_O = \frac{V_{IN}^2 \times D^2 \times \eta}{2 \times L_P \times f_S} \qquad (3)$$

In a power supply operating in the discontinuous mode, the controller will adjust the duty cycle of the primary switch to deliver enough power to the load to maintain the desired output voltage. The duty cycle is a function of both the input voltage and the output load.

Ideal Model (Continuous Mode)

Refer to Figure 7 for the characteristic waveforms for the continuous mode of operation. The reference circuit is the same as in Figure 6.

The secondary current I_{SEC} does not decay completely to zero as in the discontinuous mode, so that the third interval of operation (3) does not exist. The primary current I_{PRI} starts with a current step equal to the final value of the secondary current I_{SEC} reflected back through the transformer turns ratio. The drain to source voltage across *TOPSwitch* at the instant of turn on is also different since the third interval has been eliminated as previously discussed. The reflected output voltage state persists for the balance of the off cycle until *TOPSwitch* turns on again.

In order to maintain a constant output voltage, the amount of current ramped up in the primary inductance during the on time must be balanced by the current ramped down during the off

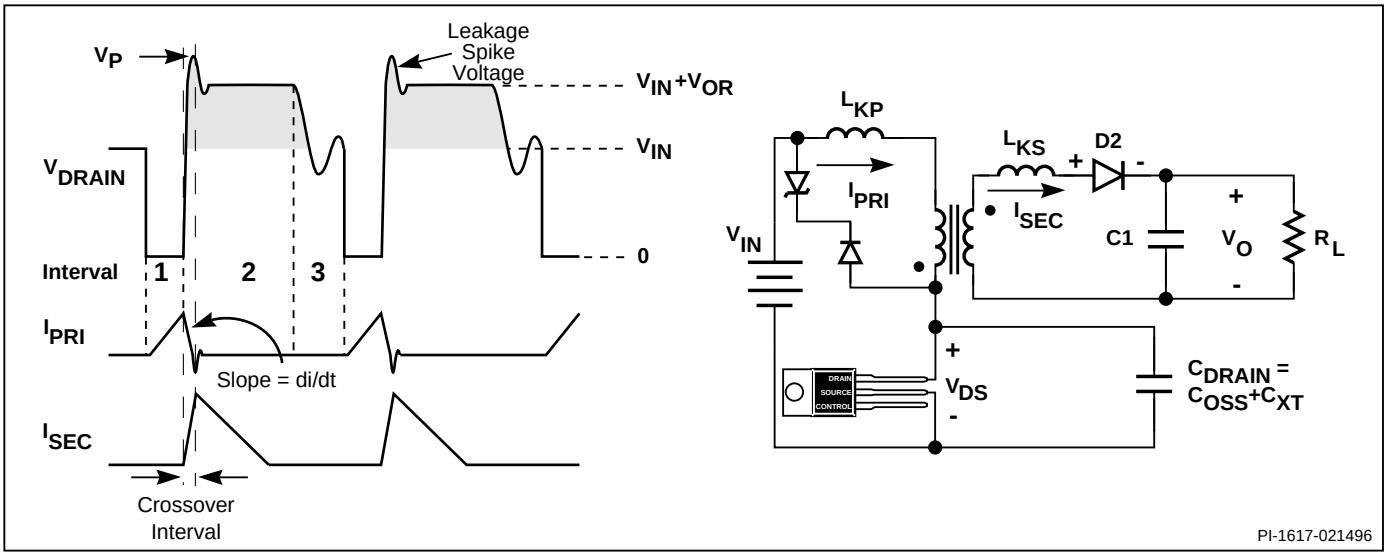

Figure 8. Non-ideal Flyback Converter Waveforms - Discontinuous Mode.

time. This means that

$$\frac{(V_{IN}-V_{DS(ON)})\times D}{L_P\times f_S}=\frac{(V_O+V_{D2})\times(1-D)}{\frac{N_S}{N_P}\times L_P\times f_S} \quad (4)$$

Solving for V_O, one obtains the expression

$$V_O=\left[(V_{IN}-V_{DS(ON)})\times\frac{D}{1-D}\times\frac{N_S}{N_P}\right]-V_{D2} \quad (5)$$

As long as the power supply is running in the continuous mode, it can be seen from the above expression that there is no direct dependence of the output voltage on the output loading. To a first order, the duty cycle of the supply will remain constant as the load is changed, and the initial value of the primary current waveform will change instead.

The primary inductance of the power transformer, output loading, and the *TOPSwitch* off time determine continuous or discontinuous operation. This dependence is shown in Equation (2). The boundary of continuous versus discontinuous operation is defined by the equation

$$I_{OB}=\frac{V_{IN}^2\times V_O}{2\times f_S\times L_P\times\left[\left(\frac{N_S}{N_P}\times V_{IN}\right)+V_O\right]^2} \quad (6)$$

Where I_{OB} is the output current at the boundary between continuous and discontinuous operation.

This equation is derived by assuming that the integral of the output current of the power supply over the entire switching cycle is exactly equal to the integral of the transformer secondary output current over the off time period. This means that during the off time, the transformer delivers exactly enough energy to balance the energy delivered to the load over the entire switching cycle, with no energy left over, and runs out exactly at the end of the off time.

If the output current is greater than the right hand side of Equation (6) , the supply is operating in the continuous mode. If the output current is less than or equal to the right hand side of the equation, the supply is operating in the discontinuous mode. A smaller transformer primary inductance will give up the energy stored in the magnetic field at a faster rate and result in discontinuous conduction mode. Conversely, a larger primary inductance will not give up all the energy stored in the core each cycle and operate in continuous mode. If the load current is reduced below I_{OB}, the supply will run in the discontinuous mode. Also, if the input voltage is increased for a given load, the supply can transition to the discontinuous mode, as I_{OB} increases with increasing input voltage.

Non-ideal Model (Discontinuous and Continuous Mode)

The circuit for the non-ideal flyback power supply and the associated waveforms for the discontinuous and continuous operating modes are shown in Figures 8 and 9. The non-ideal flyback has three additional parasitic circuit elements: two inductors and one capacitor. The inductor L_{KP} is the leakage inductance of the primary winding on the power transformer. The inductor L_{KS} is the leakage inductance of the secondary

winding on the power transformer. The capacitor C_{DRAIN} is the sum of C_{OSS} and C_{XT} which are the *TOPSwitch* output capacitance and the transformer winding capacitance, respectively. These parasitic circuit elements are present in any real-life flyback power supply circuit, and greatly affect supply performance.

As previously shown, the discontinuous mode circuit has three intervals of operation per switching cycle (see Figure 8). The impact on circuit operation of the parasitic circuit elements in each of three intervals of operation is discussed below.

In the first interval (1) the *TOPSwitch* turns on, discharging C_{OSS} and C_{XT}. The energy stored by these capacitances at the end of the previous cycle is dissipated in the *TOPSwitch* at the beginning of the turn on interval. This dissipated energy is proportional to the square of the voltage on the parasitic capacitances. Because of this effect, large values of parasitic capacitance can dramatically lower the power supply efficiency, especially at high input voltage. Leakage inductance has little effect during the turn on interval, since the transformer has no stored energy, and the initial value of the secondary output current is zero.

In interval (2) of operation, the *TOPSwitch* turns off. The energy stored in the transformer magnetic field during the previous interval is now transferred to the secondary circuit. A problem that arises during this transfer is that leakage inductances L_{KP} and L_{KS} are both trying to oppose changes in current flow. L_{KP} is trying to maintain primary current flow, and L_{KS} is trying to block secondary current flow. There is a "crossover region" during which the primary current ramps down and the secondary current ramps up. The primary current ramps down to zero with a slope determined by the value of leakage inductance and circuit voltage levels. The secondary current ramps up to the final value with a slope determined by the value of leakage inductance and circuit voltage levels. The big problem is that the primary current must continue to flow during this crossover

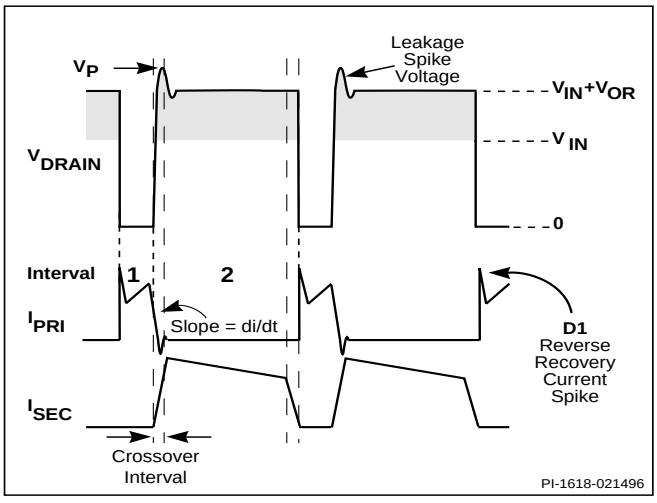

Figure 9. Non-ideal Flyback Converter Waveforms - Continuous Mode.

interval. The decaying primary current ends up flowing into C_{OSS} and C_{XT} which charge up to a peak voltage V_P. This peak voltage, caused by leakage inductance, will be referred to as the "leakage spike". In a practical *TOPSwitch* flyback supply, the leakage spike should be clamped to a value below the *TOPSwitch* breakdown voltage rating.

During interval (3) of operation, the reflected output voltage goes to zero. The transformer magnetic field has given up all the energy stored during the first interval. The *TOPSwitch* drain to source voltage makes a transition from the level equal to the sum of the reflected output voltage V_{OR} and input voltage V_{IN} down to a level equal to the input voltage V_{IN} alone. This transition excites the resonant tank circuit formed by the stray capacitance and the primary inductance to create a decaying oscillatory waveform, which persists until the *TOPSwitch* turns on again. This waveform "modulates" the voltage on (and the amount of energy stored in) C_{OSS} and C_{XT}, determining the power loss when *TOPSwitch* turns on at the beginning of the next cycle.

In the continuous mode of operation, the same parasitic elements are present as in the discontinuous mode. In addition, the non-ideal aspects of the output rectifier characteristic become important. An ideal rectifier has no forward voltage drop, and switches infinitely fast. An actual diode has a finite forward voltage drop, and takes a finite time to switch off. A PN junction diode has a finite reverse recovery time (t_{rr}) due to the fact that the minority charge carriers must be swept from the junction by the applied reverse voltage before the diode junction can reverse bias and switch to the off state. In the case of a Schottky diode, this finite recovery time is caused by junction capacitance. This recovery time (t_{rr}) is associated with a reverse recovery current spike that persists until the diode switches off. This current spike causes reverse power dissipation in the output rectifier, and loads down the *TOPSwitch* during its turn on transition. The amplitude and duration of this current spike is dependent on the speed of the diode. For 100 KHz power supplies, ultrafast diodes (trr < 50 nsec) are recommended. Use of slower diodes will cause a loss in efficiency due to excessive reverse recovery power dissipation, and can result in thermal runaway of the output rectifier diode.

Non-ideal operating waveforms of a continuous mode flyback converter are shown in Figure 9. During the interval (1) of operation, *TOPSwitch* turns on while current is still flowing in the transformer secondary. This means that the drain voltage at the instant of turn on is equal to the sum of the input voltage and the secondary voltage reflected back through the transformer turns ratio. This results in higher *TOPSwitch* turn-on power dissipation than in the discontinuous mode, due to the extra energy stored in the parasitic capacitances of the primary circuit. In addition, the current in the secondary leakage inductance must be discharged before the secondary output can be turned off. This results in a turn on current crossover while

the secondary current ramps down and the primary current ramps up. Once the secondary leakage inductance is discharged, the output rectifier D2 is reverse biased, and the charge carriers in the diode junction are withdrawn, resulting in a reverse recovery current spike that is reflected to the primary and appears at the leading edge of the primary current waveform. Depending on the diode characteristics, this initial current spike can be comparable in amplitude or higher than the final value of the primary current. This can result in spurious operation of a current limit protection circuit. The *TOPSwitch* provides built-in leading edge current limit blanking to prevent the initial current spike from spuriously triggering the current limit protection circuitry.

When *TOPSwitch* turns off, operation in the continuous mode is similar to that of the discontinuous mode. The primary and secondary current experience a crossover region due to the effects of the transformer leakage inductance. This gives rise to a primary leakage spike, as in the discontinuous operating mode. The *TOPSwitch* drain to source voltage rises to the sum of the input supply voltage and the output voltage reflected back through the transformer turns ratio. Unlike the discontinuous mode model, this reflected voltage persists until *TOPSwitch* turns on again, so that there is no interval (3) where the reflected secondary voltage decays to zero.

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