Design Example Report

Title	***<5 mW No-load Input Power, 2.1 W CV/CC Charger Using LinkZero™-LP LNK574DG***
Specification	85 VAC – 265 VAC Input; 6 V, 0.35 A Output
Application	LinkZero-LP Reference Design
Author	Applications Engineering Department
Document Number	DER-258
Date	April 29, 2013
Revision	1.3

Summary and Features

- Ultra low no-load consumption, <5 mW at 230 VAC
- Primary side CV/CC controller eliminates secondary side control and optocoupler, provides low cost, low part count solution.
- EcoSmart™ – 70% average efficiency, exceeds standards requirement of 67%, and thus meets all existing and proposed harmonized energy efficiency standards including: CECP (China), CEC, EPA, AGO, European Commission
- FEEDBACK pin reference voltage varies with output load to provide excellent cross regulation as well as cable drop compensation.
- Meets EN550022 and CISPR-22 Class B conducted EMI with 10 dB margin.

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Important Note:
Although this board was designed to satisfy safety isolation requirements, it has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the power supply.

1 Introduction

This report describes a universal input, 6 V, 350 mA flyback power supply using a LNK574DG device from the LinkZero-LP family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of important electrical waveforms.

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Figure 1 – Populated Circuit Board Photographs.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				5	mW	230 VAC
Output						
Output Voltage	V_{OUT}		6		V	See V-I Curves, Figure 9, for limits
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz bandwidth
Output Current	I_{OUT}		350		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		2.1		W	
Efficiency						
Average efficiency	η	67	70		%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55015B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge	DM	0.5			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
	CM	1			kV	
Ambient Temperature	T_{AMB}	-5		40	^{o}C	Free convection, sea level

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3 Circuit Diagram

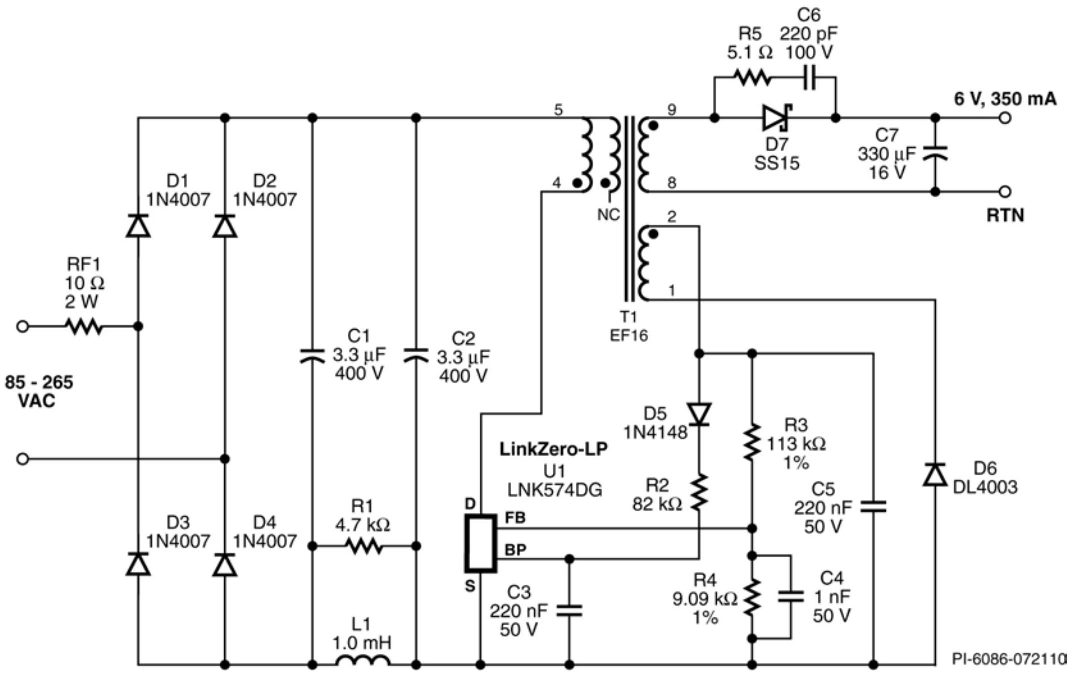

Figure 2 – Schematic.

4 Circuit Description

This flyback power supply was designed around the LNK574DG, U1 in Figure 2. The output voltage is sensed through the bias winding and fed back to U1 through resistor divider R3 and R4. That feedback is used by U1 to maintain Constant Voltage (CV) regulation of the output.

4.1 Input Rectification and Filtering

Diodes D1-D4 rectifies the AC input which is then filtered by capacitors C1 and C2. Inductor L1, C1 and C2 form a pi (π) filter that attenuates differential mode conducted EMI. Resistor R1 provides high frequency damping. Shielding techniques (E-Shield™) were used in the construction of T1 to reduce common mode EMI displacement currents. This filter arrangement, the proprietary E-Shield techniques together with the IC frequency jitter function provide excellent EMI performance even without a Y capacitor or clamp network on the primary side.

4.2 LinkZero-LP Primary

The power supply utilizes simplified bias winding voltage feedback, enabled by LNK574DG ON/OFF control. The voltage across C5 is determined by the FEEDBACK (FB) pin reference voltage and the resistor divider formed by R3 and R4. The FB pin reference voltage, which varies with load, is set to 1.36 V at no load and gradually increases to 1.70 V at full load to provide good output load regulation as well as cable drop compensation. In the CV region, U1 enables/disables switching cycles to maintain the FB pin reference voltage. Diode D6 and low cost ceramic capacitor C5 provide rectification and filtering of the primary feedback winding waveform. At increased loads, beyond the maximum power threshold, the IC transitions into the Constant Current (CC) region. In this region, the FB pin voltage begins to reduce as the power supply output voltage falls. In order to maintain a constant output current, the internal oscillator frequency is reduced in this region until it reaches typically 48% of the starting frequency. When the FB pin voltage drops below the auto-restart threshold (typically 0.9 V on the FB pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for 1.2 s and then turn back on for 170 ms. The auto-restart function reduces the average output current during an output short-circuit condition.

4.3 Design of External Bias for LinkZero-LP

Diode D5 and R2 form the external bias circuit and although this is not necessary for the operation of the LinkZero-LP family, its use can help to significantly improve the average efficiency of a power supply, especially at 230 VAC. During steady-state operation the external bias circuit supplies the IC bias current. Resistor R2 is chosen such that the bias winding supplies 200 μA to 300 μA into the BP pin.

4.4 Primary Clamp and Transformer Construction

A clampless primary circuit is achieved due to the very tight tolerance current limit trimming techniques used in manufacturing the LNK574DG, plus the transformer construction techniques used. Peak drain voltage is therefore limited to typically less than

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550 V at 265 VAC – providing significant margin to the 700 V maximum drain voltage (BV_{DSS}).

4.5 Output Rectification

Output rectification is provided by diode D7 and filtering is provided by capacitor C7. Resistor R5 and capacitor C6 provide high frequency filtering for improved EMI.

4.6 Ultra-low No-load Input Power

The LinkZero-LP has a built in “power-down” (PD) mode wherein when 160 consecutive switching cycles have been skipped, the chip goes into the PD mode and inhibits switching and in addition, dramatically reduces its internal power consumption. The PD mode occurs when the output load has reduced to about 0.3% of full load. During PD mode the internal circuitry of the device completely shuts down and thus the capacitor connected to BYPASS (BP) pin C3 is discharged from 5.8 V. The controller wakes up to check output load conditions at a frequency determined by the user through the choice of the BP pin capacitor value. Once the BP pin voltage reaches 3 V, U1 powers up again and resumes switching. The no-load power consumption can be reduced further with a higher value for BP pin capacitor C3. If the load increases such that fewer than 160 cycles were skipped, the IC resumes normal operation.

When U1 is in PD mode, the time taken for the BP pin voltage to discharge to VBPPDRESET (~3 V) determines the duration of the PD off-time. The duration of the PD off-time also determines the ripple on the output voltage. The total energy stored in C5 and C3 determine the PD off-time (and also the output ripple in PD mode). The typical choice for C5 is between 100 nF and 330 nF and for C3 is between 47 nF and 470 nF.

5 PCB Layout

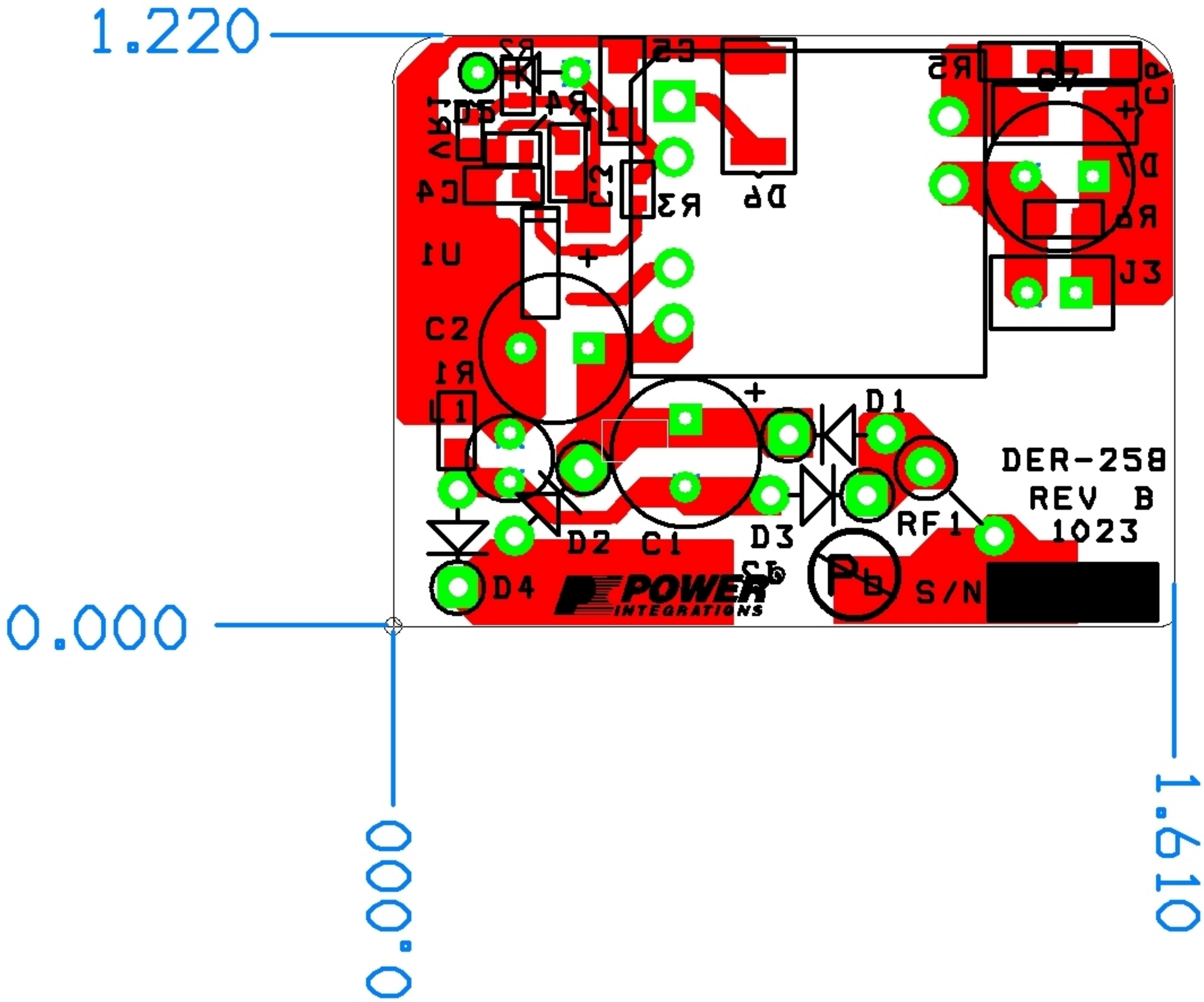

Figure 3 – Printed Circuit Board Layout (Dimensions in Inches).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer P/N	Manufacturer
1	2	C1 C2	3.3 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G3R3MK0811MLL3	Taicon
2	1	C3	220 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H224KA01L	Murata
3	1	C4	1000 pF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H102K	Panasonic
4	1	C5	220 nF, 50 V, Ceramic, X7R, 1206	ECJ-3YB1H224K	Panasonic
5	1	C6	220 pF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A221K	Panasonic
6	1	C7	330 μF, 16 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE160ELL331MHB5D	Nippon Chemi-Con
7	4	D1 D2 D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
8	1	D5	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
9	1	D6	200 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4003-13-F	Diodes Inc
10	1	D7	50 V, 1 A, Schottky, DO-214AC	SS15-TP	Micro commercial
11	1	J3	6 ft, 26 AWG, 2.1 mm connector (custom)	3PH323A0	Anam
12	1	L1	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
13	1	R1	4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
14	1	R2	82 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ823V	Panasonic
15	1	R3	113 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1133V	Panasonic
16	1	R4	9.09 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9091V	Panasonic
17	1	R5	5.1 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R1V	Panasonic
19	1	RF1	10 Ω, 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 10R	Vitrohm
20	1	T1	Bobbin, EF16, Horizontal, 9 pins (5x4)	EF16HP09-QO	TDK
21	1	U1	LinkZero-LP, SO-8	LNK574DG	Power Integrations

Note – All parts are RoHS compliant

7 Transformer Specification

7.1 Electrical Diagram

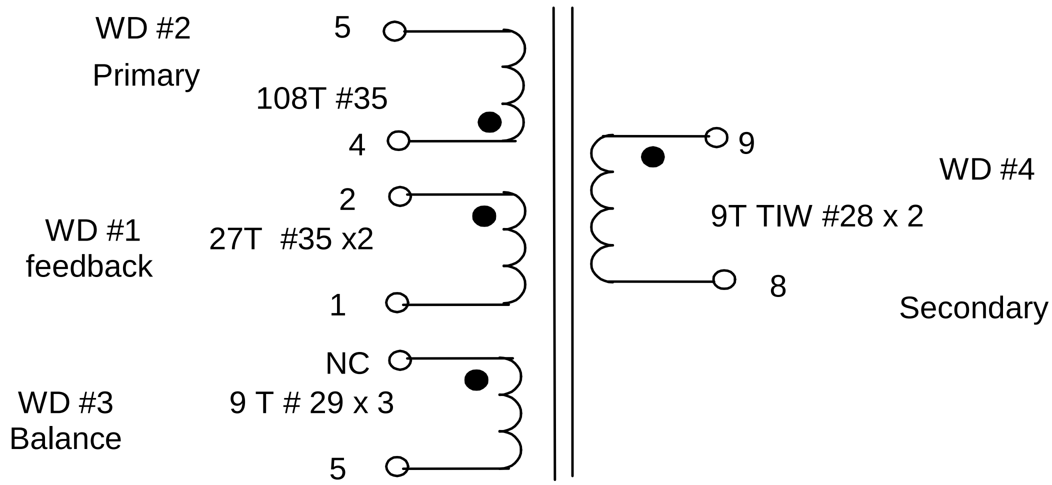

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-9.	3000 VAC
Primary Inductance	Pins 5-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	2.75 mH, ±10%
Resonant Frequency	Pins 5-4, all other windings open.	520 kHz (Min.)
Primary Leakage Inductance	Pins 4-5, with pins 7-9 shorted, measured at 100 kHz, 0.4 V_{RMS}.	50 μH (Max.)

7.3 Materials

Item	Description
[1]	Core: PC44 EF16-Z, TDK or equivalent gapped for AL of 235.8 nH/T^2
[2]	Bobbin: EE16X16H, Horizontal 9 pin
[3]	Magnet Wire: #35 AWG
[4]	Magnet Wire: #29 AWG
[5]	Triple Insulated Wire: #28 AWG
[6]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 9.8 mm wide
[7]	Varnish

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7.4 Transformer Build Diagram

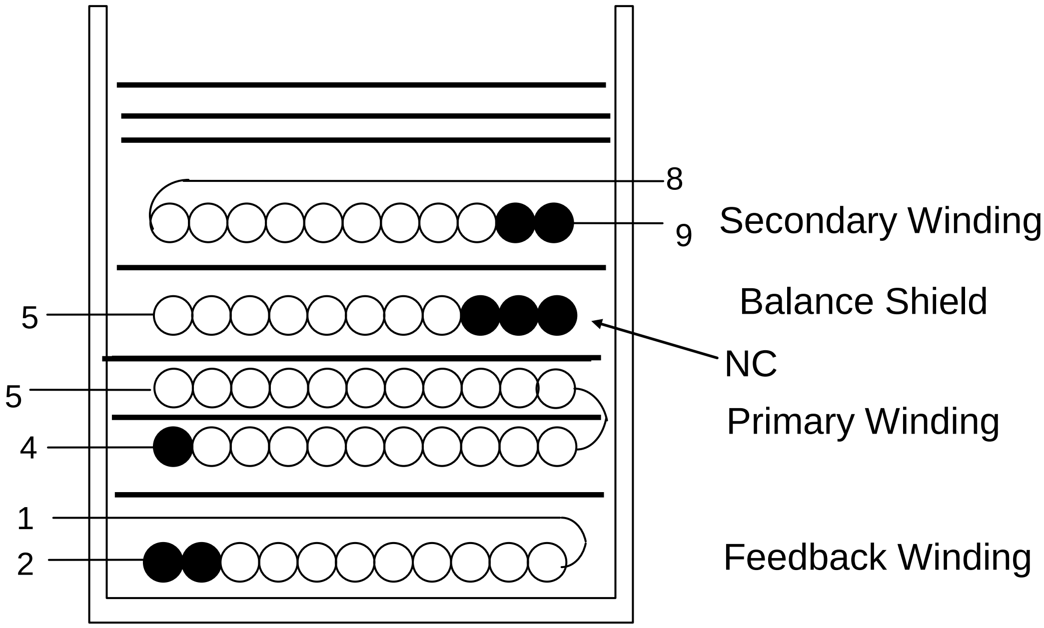

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Primary pin side of the bobbin orients to the left hand side.
WD#1 Feedback	Start on pin 2, wind 27 bifilar turns of item [3] from left to right. Wind with tight tension across entire bobbin evenly. Finish on pin 1.
Insulation	1 layer of tape [6] for insulation
WD#2 Primary	Start on pin 4, wind 54 turns of item [3] from left to right. After finishing the first layer, placing one layer of tape [6]. Continue to wind the wire from right to left with another 54 turns. Finish on pin 5.
Insulation	1 layer of tape [6] for insulation.
WD #3 Balance Shield	Start on any pin on the secondary temporarily. Wind 9 trifilar turns of item [4], wind from right to left with tight tension uniformly, and connect end of winding to pin 5. Cut out wire connected to secondary side and leave this end not connected
Insulation	1 layer of tape [6] for insulation.
WD #4 Secondary	Start at pin 9, wind 9 bifilar turns of item [5] from right to left. Wind uniformly. After finishing the 9^{th} turn, bring the wire back and finish it on pin 8.
Insulation	3 layers of tape [6] for insulation.
Grind Core	Grind the core to get 2.75 mH. Secure the core with tape.
Secure and Varnish	Secure the core with tape. Dip varnish for 3 minutes.

8 Transformer Design Spreadsheet

LinkZero-LP 052410; Rev.1.0; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	LinkZero-LP 052410_Rev1-0.xls; LinkZero-LP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	6.00			Volts	Output Voltage (main) measured at the end of output cable (For CV/CC designs enter typical CV tolerance limit)
IO	0.32			Amps	Power Supply Output Current (For CV/CC designs enter typical CC tolerance limit)
PO			1.92	Watts	Output Power (VO x IO + dissipation in output cable)
Feedback Type	BIAS		Bias Winding		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Clampless design	YES		Clampless		Choose 'YES' from the 'Clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply
N	0.70		0.7		Efficiency Estimate at output terminals. For CV only designs enter 0.7 if no better data available
Z	0.45		0.45		Loss Allocation Factor (Secondary side losses / Total losses)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	10.00			uFarads	Input Capacitance
Input Rectification Type	F		**F**		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkZero-LP VARIABLES					
LinkZero-LP	**Auto**		**LNK574**		LinkZero-LP device.
Chosen Device		LNK574			
ILIMITMIN			0.126	Amps	Minimum Current Limit
ILIMITMAX			0.146	Amps	Maximum Current Limit
fSmin			93000	Hertz	Minimum Device Switching Frequency
I^2fMIN			1664.64	A^2Hz	I^2f Minimum value (product of current limit squared and frequency is trimmed for tighter tolerance)
I^2fTYP			1849.6	A^2Hz	I^2f typical value (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	78.00		78	Volts	Reflected Output Voltage
VDS			10	Volts	LinkZero-LP on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			1.60		Ripple to Peak Current Ratio (0.9<KRP<1.0 : 1.0<KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EF16**		**EF16**		User-Selected transformer core
Core		EF16		P/N:	PC40EF16-Z
Bobbin		EF16_BOBBIN		P/N:	EF16_BOBBIN
AE			0.201	cm^2	Core Effective Cross Sectional Area
LE			3.76	cm	Core Effective Path Length
AL			1100	nH/T^2	Ungapped Core Effective Inductance
BW			10	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of primary layers
NS	9		9		Number of Secondary Turns
NB			28		Number of Bias winding turns

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VB			19.50	Volts	Bias Winding Voltage
R1			113.00	k-ohms	Upper Resistor in the resistor divider component between bias wiinding and FB pin of LinkZero-LP
R2			8.87	k-ohms	Lower Resistor in the resistor divider component between bias wiinding and FB pin of LinkZero-LP
RBP			86.6	k-ohms	Optional BP pin resistor (connected between BP pin and bias winidng) to improve efficiency
CFB			680.00	pF	FB pin resistor (Improve noise sensitivity)
CBP			220.00	nF	BP pin capacitor
Recommended Bias Diode			1N4003		Place this diode on the return leg of the bias winding for optimal EMI.
DC INPUT VOLTAGE PARAMETERS					
VMIN			103	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.37		Maximum Duty Cycle
IAVG			0.03	Amps	Average Primary Current
IP			0.1260	Amps	Minimum Peak Primary Current
IR			0.1260	Amps	Primary Ripple Current
IRMS			0.05	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2724	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			108		Primary Winding Number of Turns
ALG			234	nH/T^2	Gapped Core Effective Inductance
BM			1832	Gauss	Maximum Operating Flux Density, BM<2000 is recommended
BAC			916	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1637		Relative Permeability of Ungapped Core
LG			0.10	mm	!!! Info. Gap sizes below 0.1 mm may cause manufacturing tolerancing problems - please verify with magnetics vendor. Increase LG > 0.1 mm (increase NS, decrease VOR,bigger Core)
BWE			20	mm	Effective Bobbin Width
OD			0.185	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.145	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32	Cmils	Bare conductor effective area in circular mils
CMA		*Info*	676	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L(primary layers),increase NS,use smaller Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.51	Amps	Peak Secondary Current
ISRMS			0.62	Amps	Secondary RMS Current
IRIPPLE			0.53	Amps	Output Capacitor RMS Ripple Current
CMS			124	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			29	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.11	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.41	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			-	Volts	Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.
PIVS			37	Volts	Output Rectifier Maximum Peak Inverse Voltage

9 Performance Data

The ON/OFF control scheme employed by LinkZero-LP helps to yield virtually constant efficiency across the 25% to 100% load range required for compliance with EPA, CEC, CECP and AGO energy efficiency standards for external power supplies (EPS). This performance is automatic with ON/OFF control. There are no special burst modes that require the designer to consider specific thresholds within the load range in order to achieve compliance with global energy efficiency standards.

All measurements performed at room temperature, 50 Hz input frequency.

9.1 Efficiency

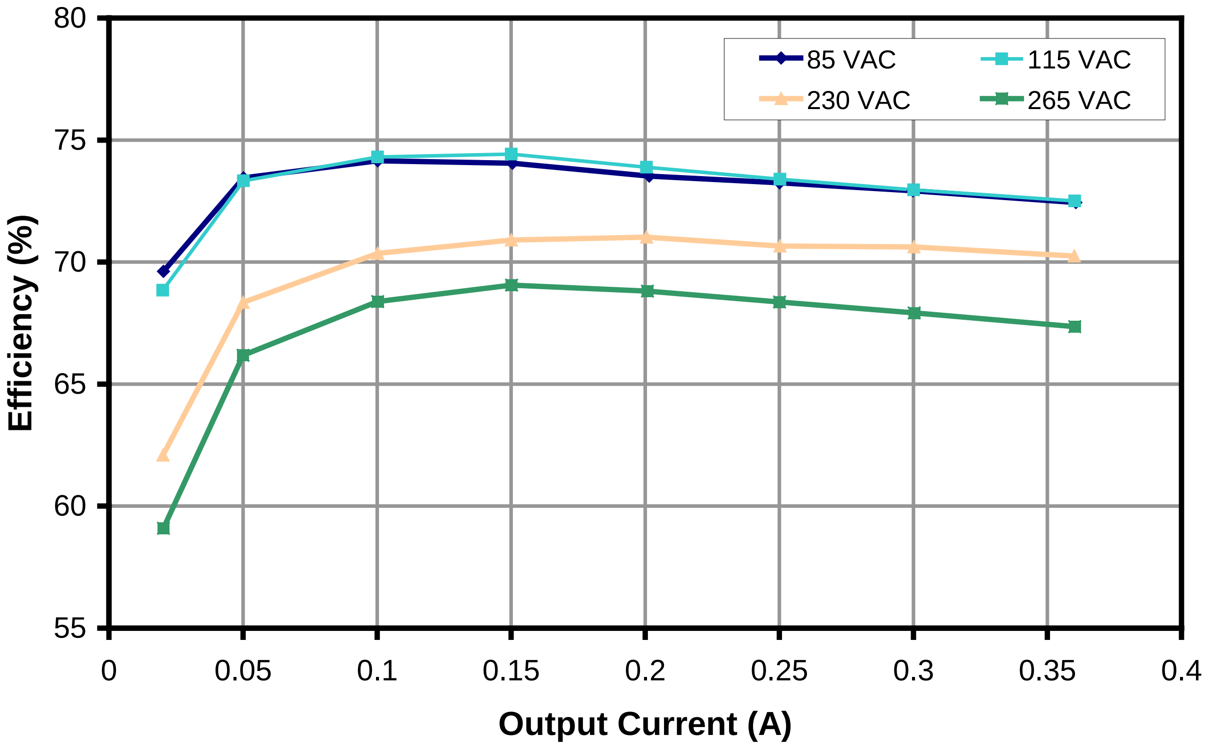

Figure 6 – Efficiency vs. Output Current, Room Temperature, 60 Hz.

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Percent of Full Load	Efficiency (%)	
	115 VAC	**230 VAC**
25	74.9	68.9
50	74.6	70.0
75	73.7	70.9
100	72.9	70.2
Average	74.0	70.0
US EISA (2007) requirement	**57**	
ENERGY STAR 2.0 requirement	**67**	

9.2 Active Mode CEC Measurement Data

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
$\geq$ 1 W to $\leq$ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	$\leq$ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
$\leq$ 1 W	$0.48 \times P_O + 0.14$
> 1 W to $\leq$ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq$ 550 mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
$\leq$ 1 W	$0.497 \times P_O + 0.067$
> 1 W to $\leq$ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	$\leq$ 0.3 W
$\geq$ 50 W to $\leq$ 250 W	$\leq$ 0.5 W

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9.3 No-load Input Power

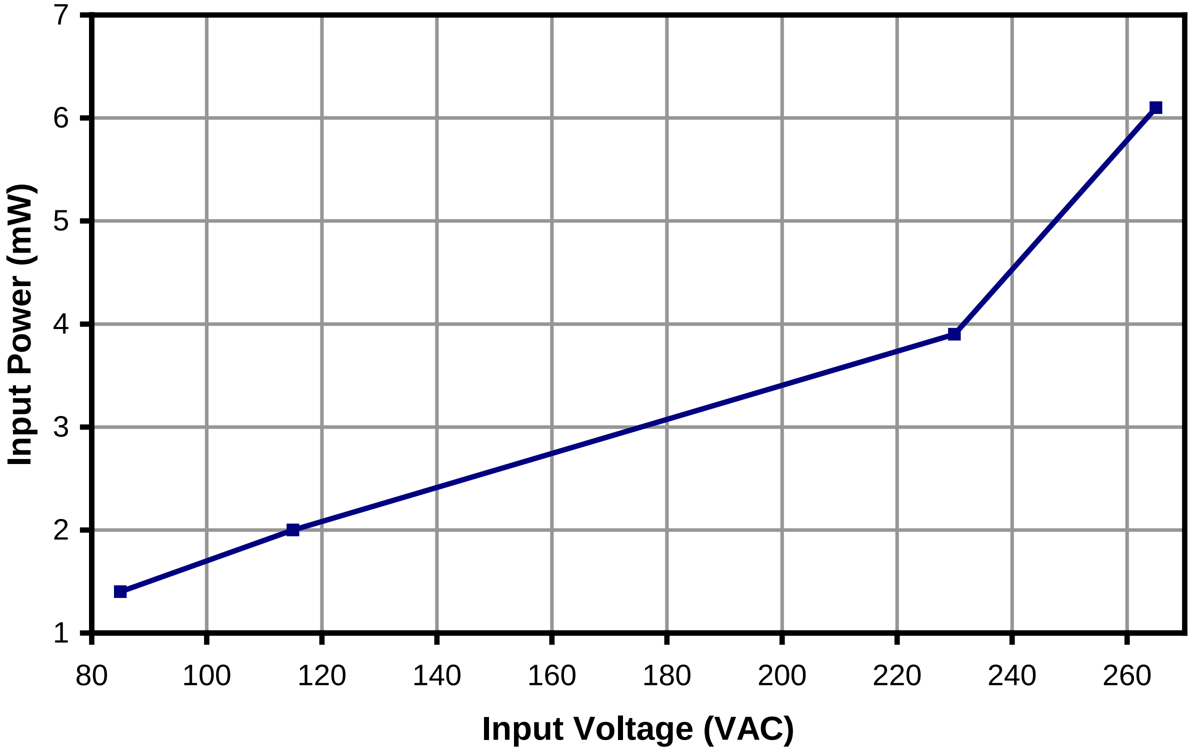

Figure 7 – No-load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 0.3 W, 0.5 W, 1 W and 2 W.

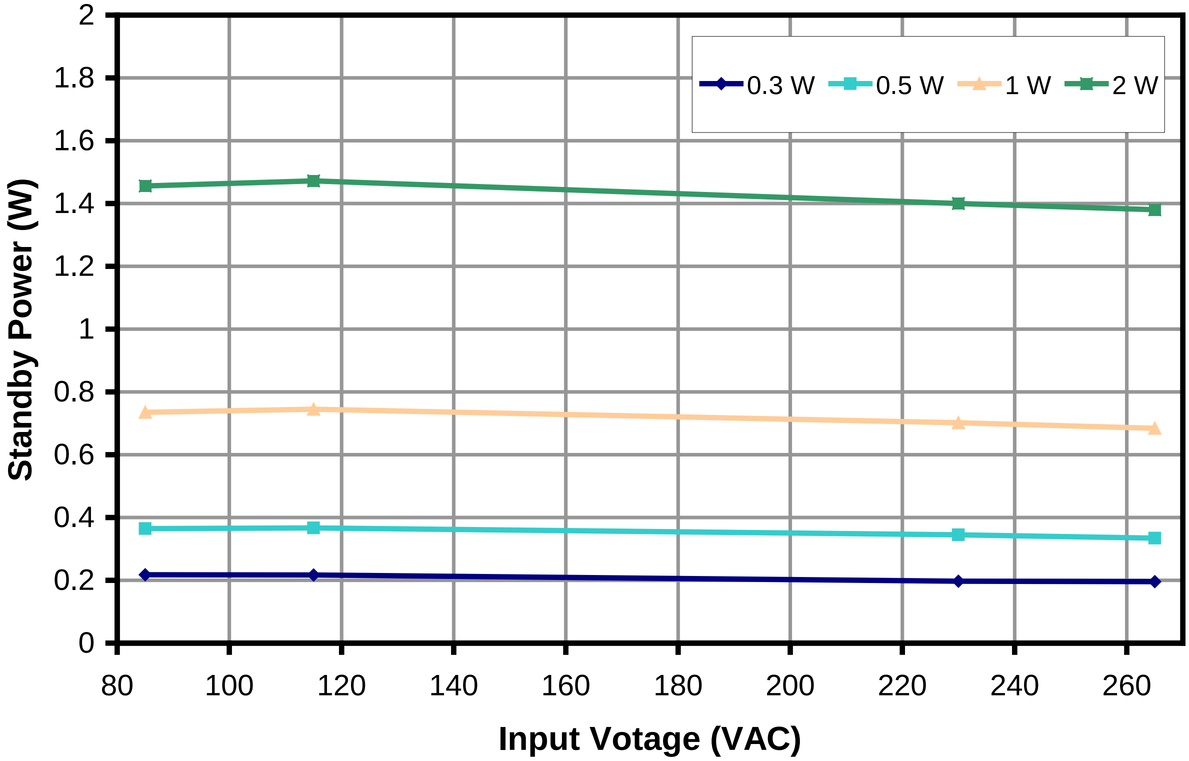

Figure 8 – Available Output Power for 0.2 W, 0.5 W, 1 W and 2 W Input Power.

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9.5 Line and Load Regulation

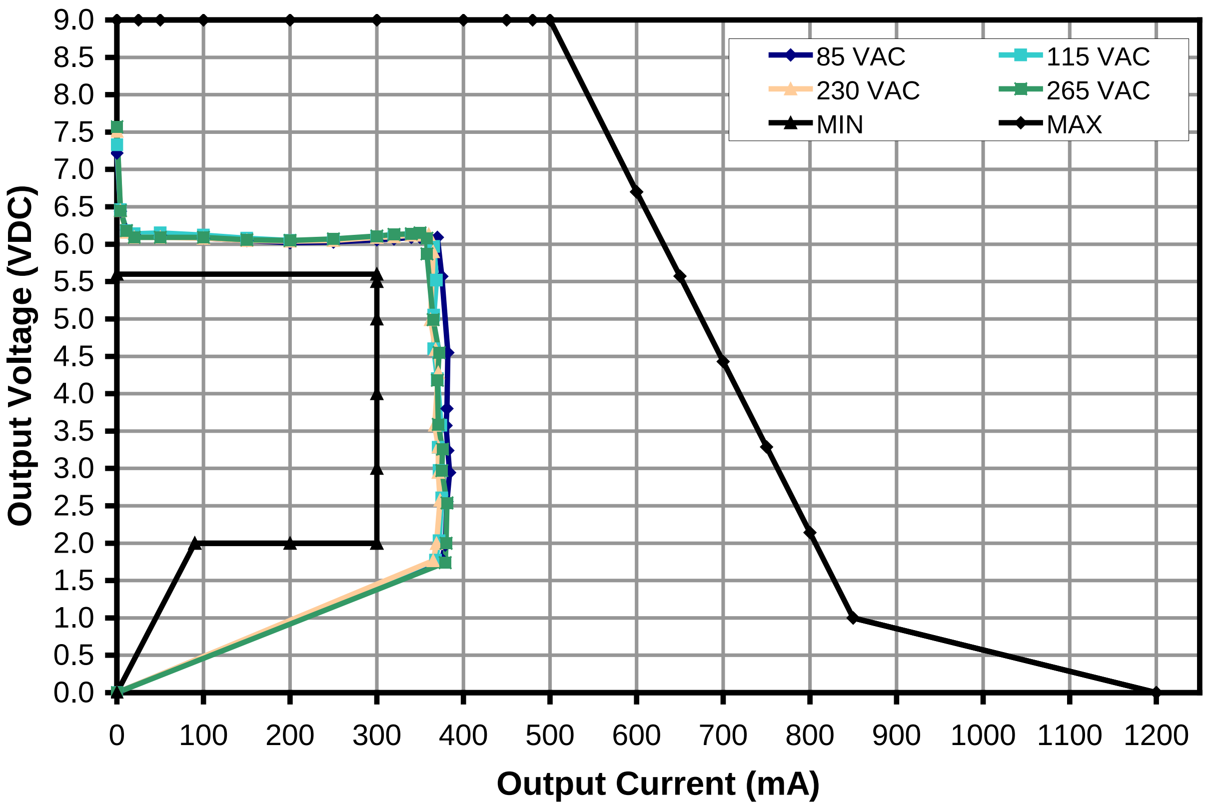

Figure 9 – Load and Line Regulation, Room Temperature.

10 Thermal Performance

Temperature measurements of key components were taken using T-type thermocouples. The thermocouples were soldered directly to a SOURCE pin of the LNK574DG device and to the cathode of the output rectifier D7. The thermocouples were glued to the external core and winding surfaces of transformer T1.

Item	Temperature °C	
	85 VAC	265 VAC
Ambient Inside Box*	51.0	51.0
LNK574DG	72.0	90.0
Transformer	70.0	73.0
Output Diode	63.0	67.0

*To simulate operation inside sealed enclosure at 40 °C external ambient.

These results show that all the parts in the board have thermal margin to run at 50 ºC ambient.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

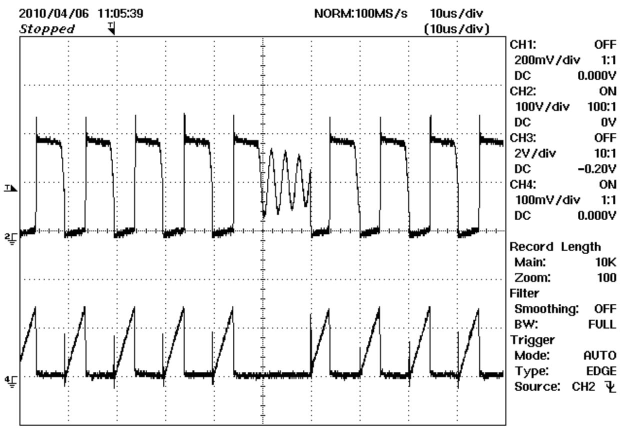


Figure 10 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div. (MAX DRAIN VOLTAGE = 250 V).
Lower: I_{DRAIN}, 0.1 A, 10 μs / div.

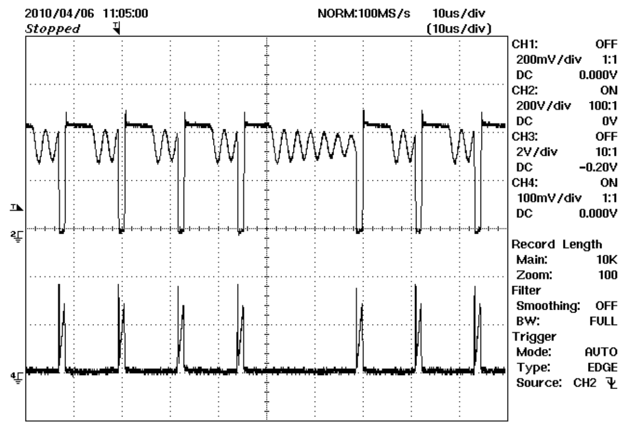


Figure 11 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div. (MAX DRAIN VOLTAGE = 500 V).
Lower: I_{DRAIN}, 0.1 A, 10 μs / div.

11.2 Output Voltage Start-Up Profile

Start-up into full resistive load and no-load were both verified. An 18 Ω resistor was used for the load, to maintain a 0.35 A under steady-state conditions.

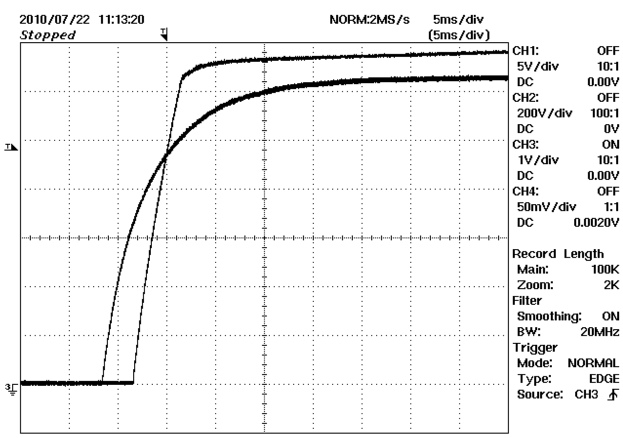


Figure 12 – Start-Up Profile, 115 VAC.
Fast Trace is at No-load.
Slower Trace is at Maximum Load.
1 V, 5 ms / div.

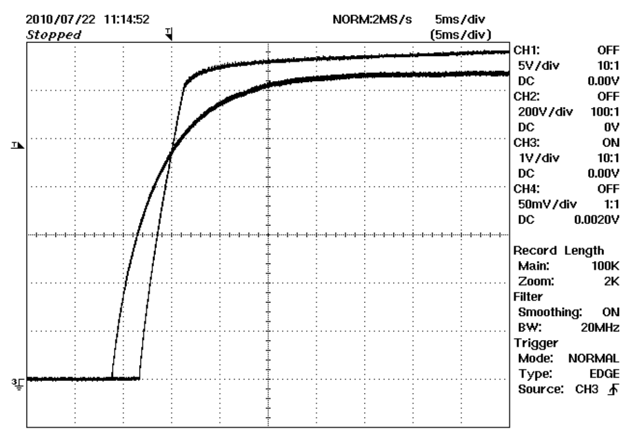


Figure 13 – Start-Up Profile, 230 VAC.
Fast Trace is at No-load.
Slower Trace is at Maximum Load.
1 V, 5 ms / div.

11.3 Drain Voltage and Current Start-Up Profile

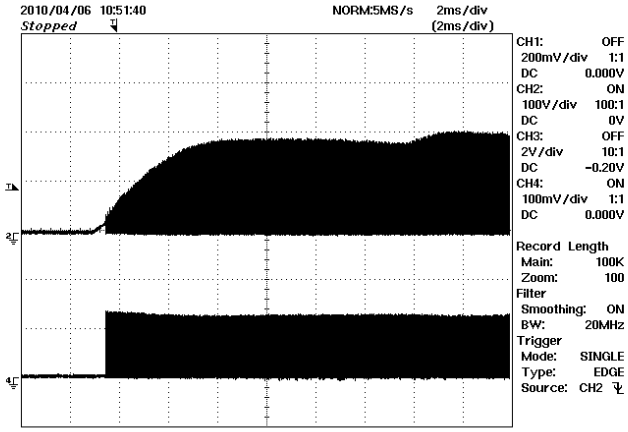


Figure 14 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.1 A, 1 ms / div.

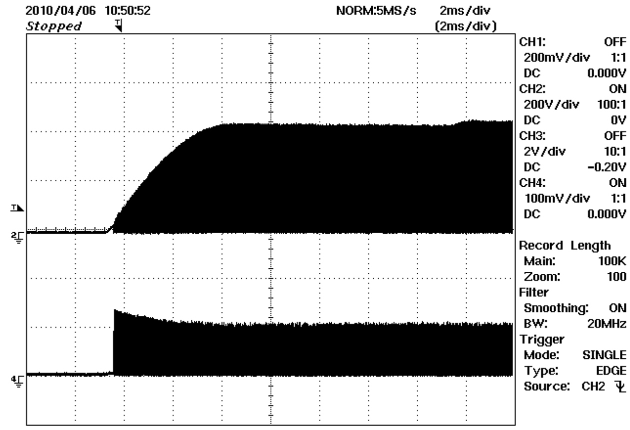


Figure 15 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.1 A, 1 ms / div.

11.4 Load Transient Response

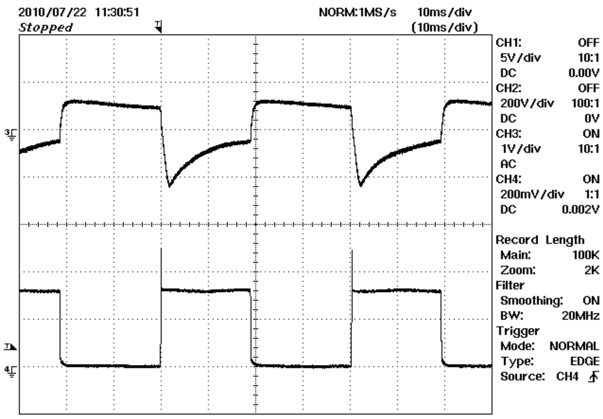


Figure 16 – Transient Response, 115 VAC, 2 mA to 350 mA to 2 mA. Upper: V_{OUT} 1 V / div. Lower: I_{OUT} 0.2 A, 10 ms / div.

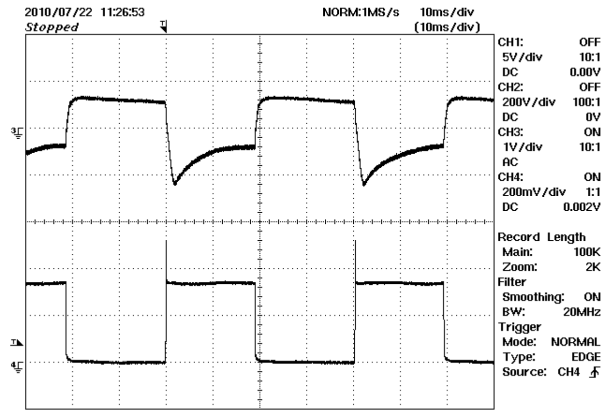


Figure 17 – Transient Response, 230 VAC, 2 mA to 350 mA to 2 mA. Upper: V_{OUT} 1 V / div. Lower: I_{OUT} 0.2 A, 10 ms / div.

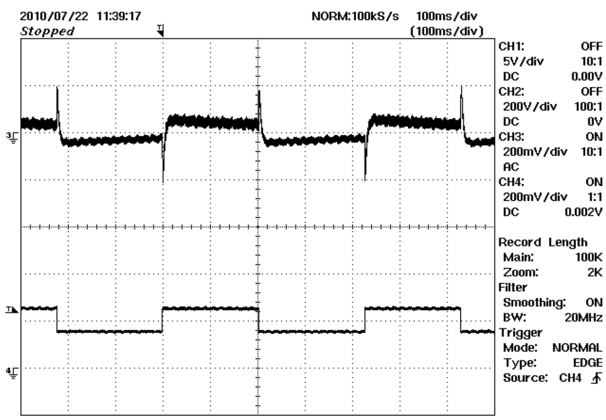


Figure 18 – Transient Response, 115 VAC, 170 mA to 262 mA to 170 mA. Upper: V_{OUT} 0.2 V / div. Lower: I_{OUT} 0.2 A, 10 ms / div.

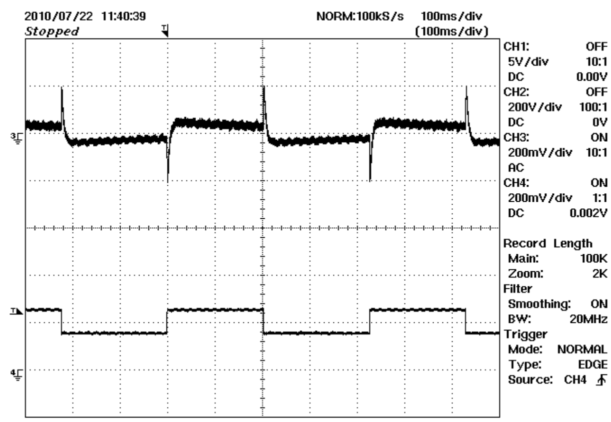
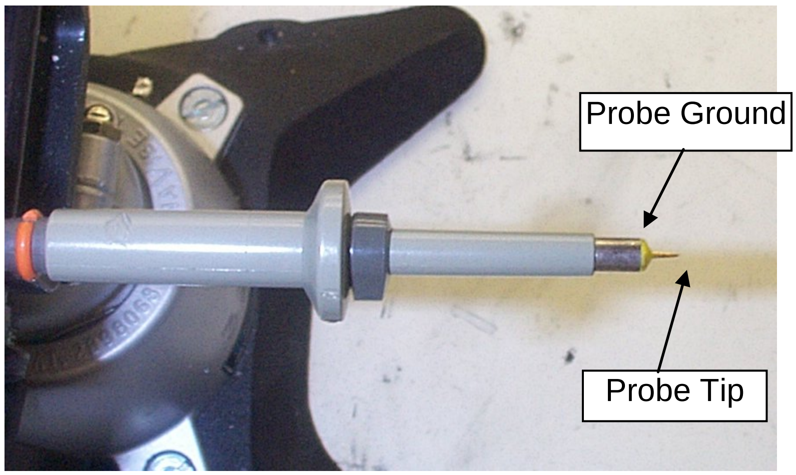


Figure 19 – Transient Response, 230 VAC, 170 mA to 262 mA to 170 mA. Upper: V_{OUT} 0.2 V / div. Lower: I_{OUT} 0.2 A, 10 ms / div.

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

A modified oscilloscope test probe was used to take output ripple measurements, in order to reduce the pickup of spurious signals. Using the probe adapter pictured below, the output ripple was measured with a 1 μF electrolytic, and a 0.1 μF ceramic capacitor connected as shown.



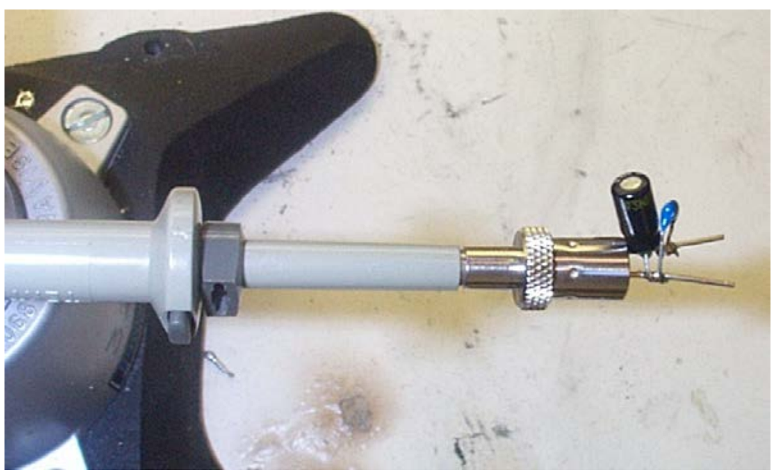


Figure 20 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

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11.5.2 Measurement Results

The maximum voltage ripple at the output terminals of the power supply was measured as 80 mV, well below 200 mV specification limit.

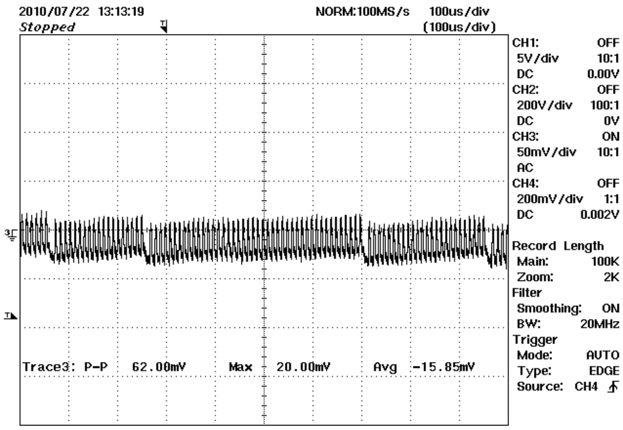

Figure 21 – Ripple, 85 VAC, Full Load.
100 µs, 50 mV / div.

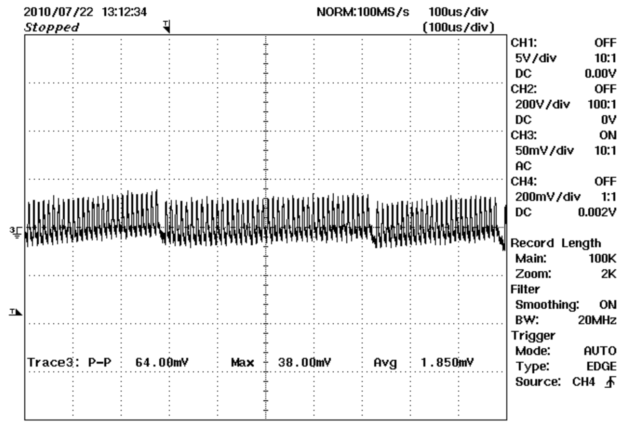

Figure 22 – Ripple, 115 VAC, Full Load.
20 µs, 50 mV / div.

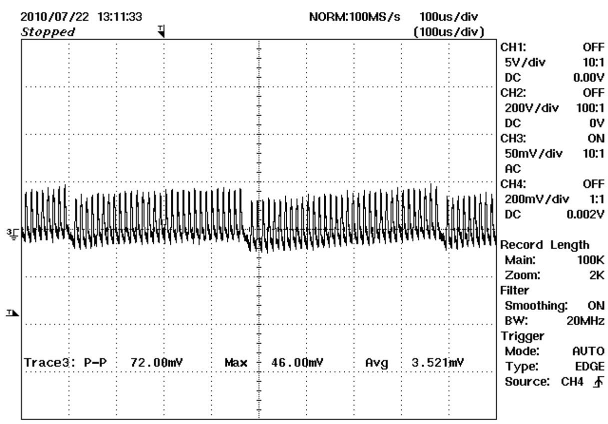

Figure 23 – Ripple, 230 VAC, Full Load.
100 µs, 50 mV / div.

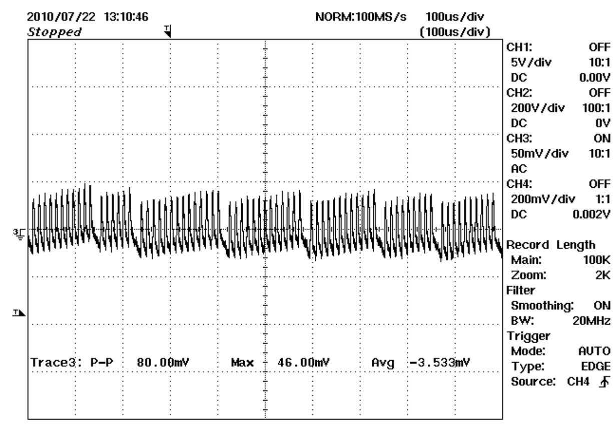

Figure 24 – Ripple, 265 VAC, Full Load.
100 µs, 50 mV / div.

12 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at maximum load. Measurements were taken with an Artificial Hand connected to a load resistor. EMI of line and neutral were scanned into one picture and the load resistance was adjusted for maximum power output.

Composite EN55022B / CISPR22B conducted limits are shown. In all cases there was excellent (~10 dB) margin.

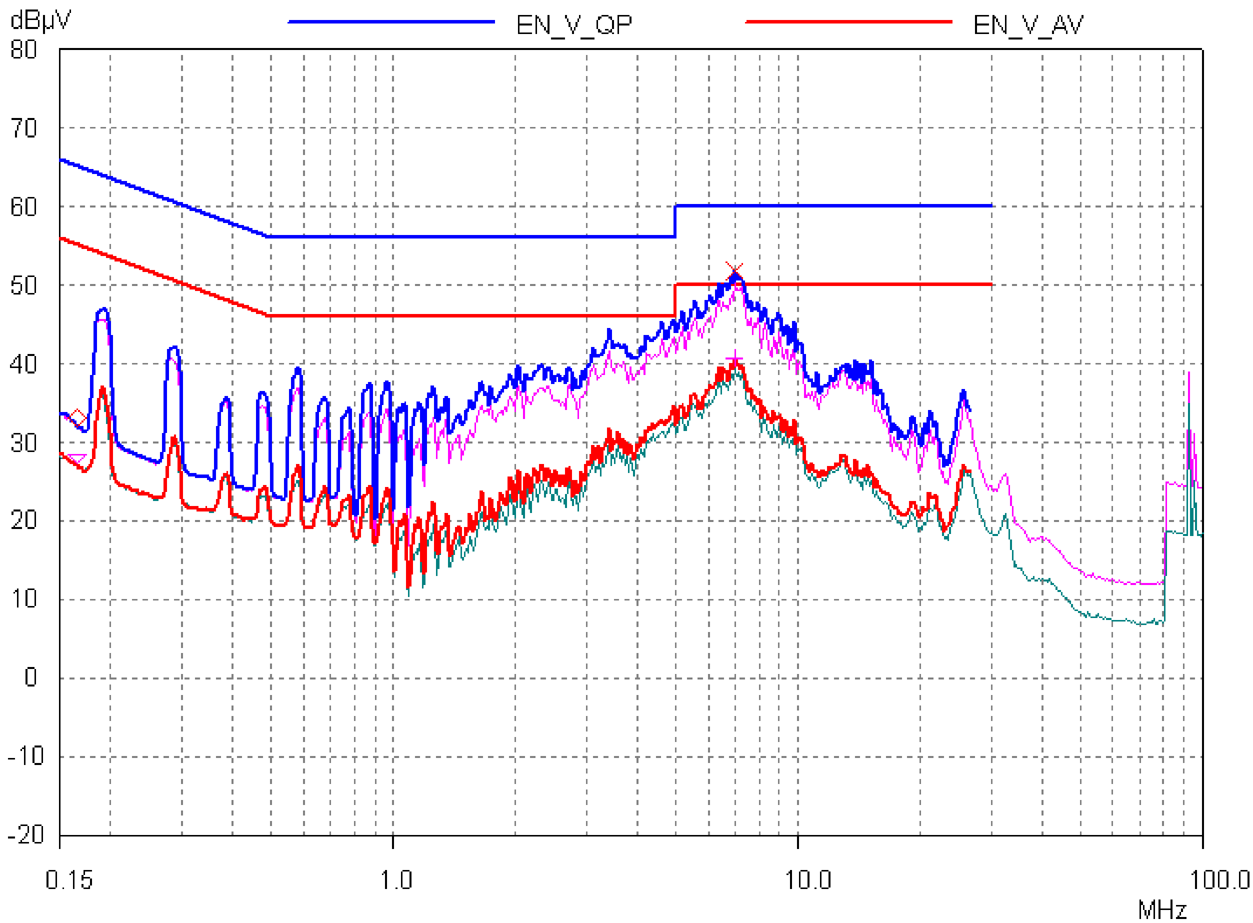

Figure 25 – Conducted EMI at 115 VAC, Artificial Hand, 6.2 V, 0.362 A.

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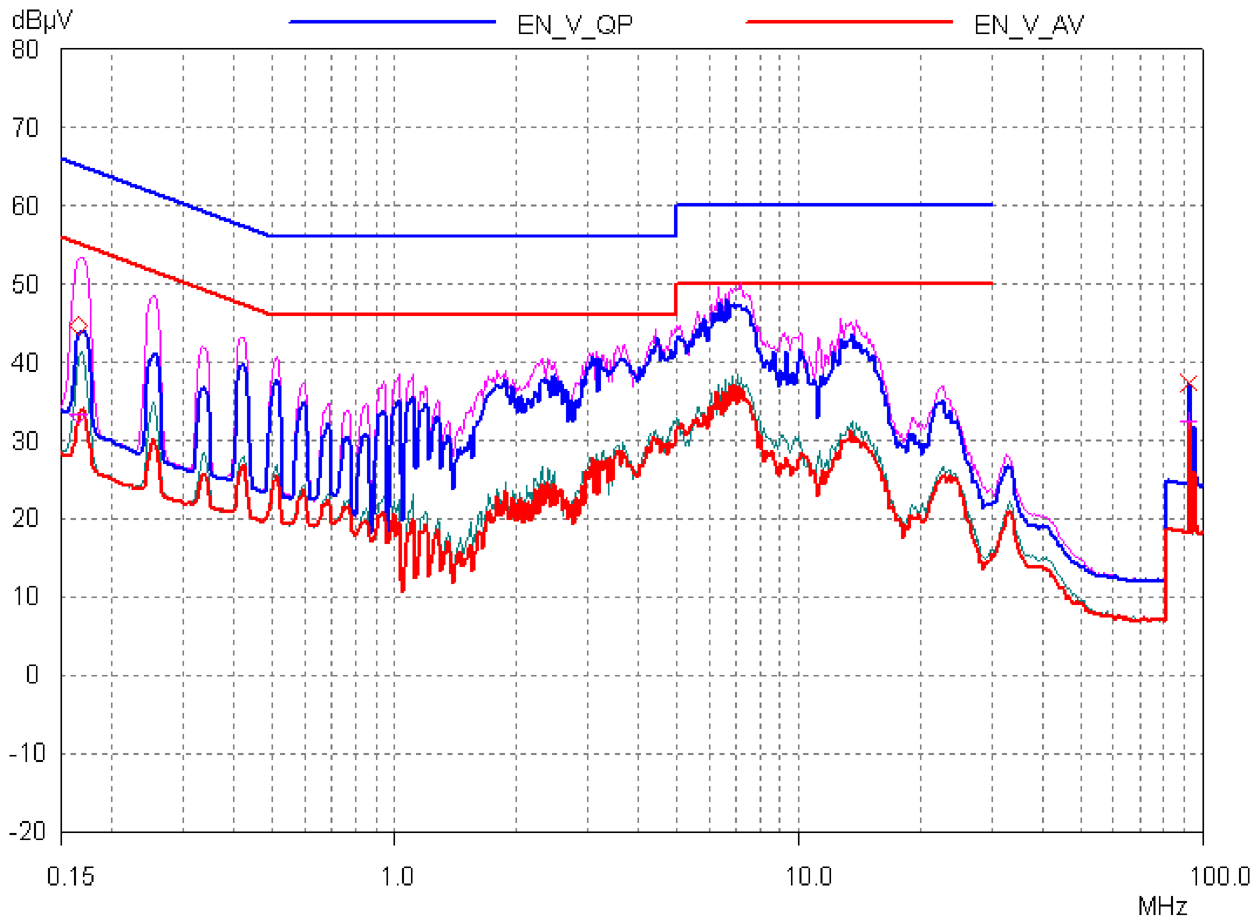

Figure 26 – Conducted EMI at 230 VAC, Artificial Hand, 6.05 V, 0.373 A.

13 Statistical Data for the Design

The following is some statistical data collected from 50 DER-258 design boards to demonstrate the repeatability and variation of certain measurements over a relatively large sample size, line voltage and temperature.

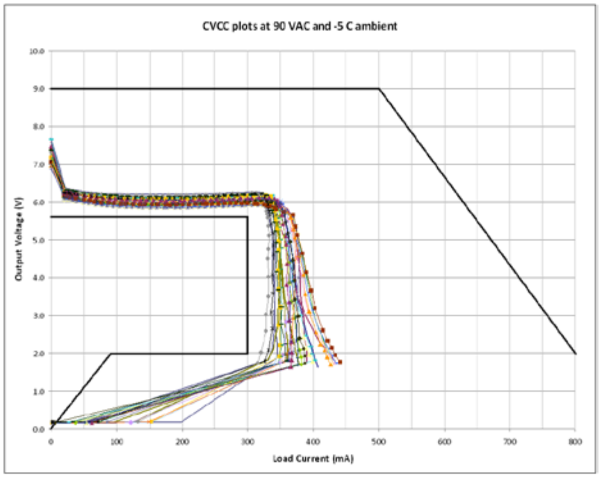

Figure 27 – Cold Temperature Regulation. CVCC Response Measured at -5 ºC and 90 VAC.

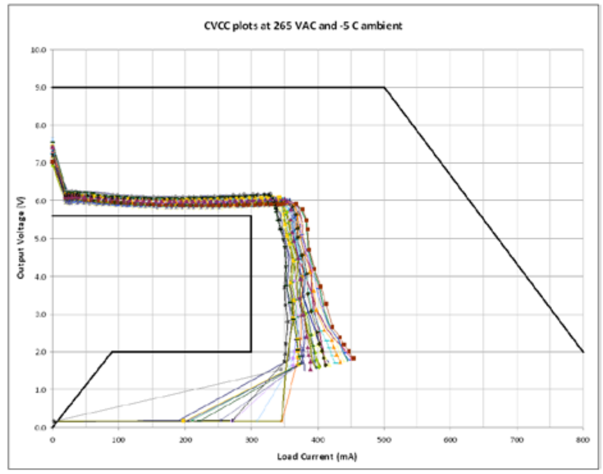

Figure 28 – Cold Temperature Regulation. CVCC Response Measured at -5 ºC and 265 VAC.

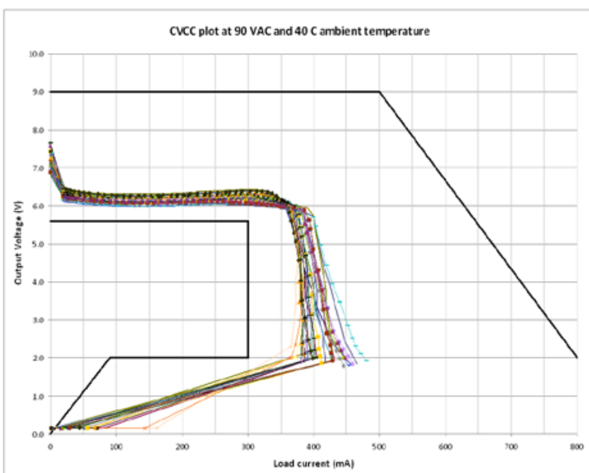

Figure 29 – High Ambient Regulation. CVCC Response Measured at 40 ºC and 90 VAC.

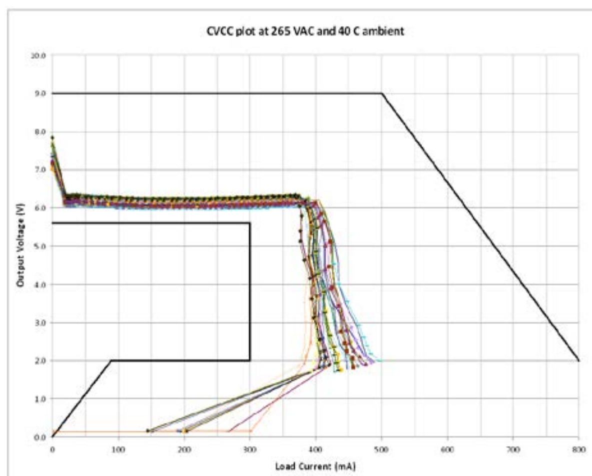

Figure 30 – High Ambient Regulation. CVCC Response Measured at 40 ºC and 265 VAC.

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
07-Dec-10	PL	1.2	Initial Release	Apps and Mktg
29-Apr-13	KM	1.3	Updated Board Photos	

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