



Design Example Report

Title	<i>Lossless Generation of AC Zero Crossing and AC Fault/Loss Signals using CAPZero™</i>
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Summary

- Circuits providing zero crossing/line frequency and AC fault/loss signals are presented
 - These circuits address isolated and non-isolated systems with both positive and negative output voltages
- Signals are generated using lossless circuit configurations
 - All circuits use the existing CAPZero supply current to generate signals
 - Consumption related to zero crossing/line frequency and AC line fault/loss signal generation is therefore eliminated

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1 Introduction

Energy efficiency regulations such as the European ErP Lot 6 specification are demanding very low power consumption under standby and operating conditions. It is therefore now important to eliminate the energy consumption associated with high-voltage resistor dividers of the type typically used for zero crossing (ZC) and AC line loss detection signal generation.

This report describes circuits employing CAPZero that provide zero crossing/line frequency and AC Loss information whilst also providing the normal CAPZero X capacitor discharge function with no additional power consumption. The system schematics used in the report highlight the circuitry specific to generating the ZC and AC Loss signals.

Since typical applications can be both isolated and non-isolated with positive and negative output voltages, a variety of circuit configurations are described in the following sections to cover many typical applications.

Simplified schematics and waveforms are presented at the start of each section to illustrate the system configuration being discussed. Using the principles introduced in this report, configurations other than those shown can be designed employing CAPZero to provide Zero Crossing and AC Loss signals in other system configurations.

CAPZero basics are covered first, followed by lossless zero crossing circuits and final the use of these zero crossing signals to generate AC Loss signals is discussed

Throughout the report, statements that power consumption is eliminated or that circuits are lossless, use the IEC 62301 clause 4.5 definition of zero power as a consumption of less than 5 mW.

2 CAPZero Basics

Figure 1 shows the typical application and selection tables from the CAPZero data sheet.

CAPZero, R1 and R2 consume <5 mW from the AC input while the AC voltage supply is connected. However, when the AC is disconnected, the resistors R1 and R2 are connected together through CAPZero to provide the normal X capacitor discharge as required by international safety standards.

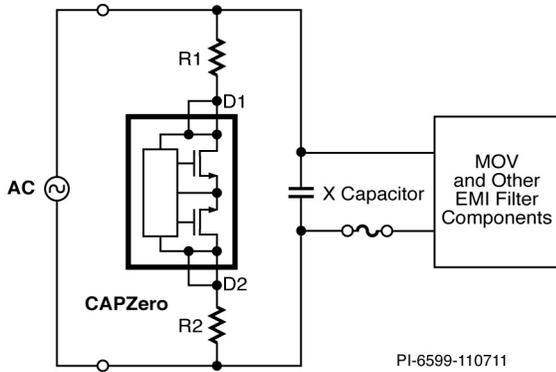
To achieve <5 mW consumption, the CAPZero supply current is <21.7 μ A from the AC line while the AC voltage is connected. It is this supply current that is used by the external circuits described in this report to generate the ZC or AC line loss/fault signals.

This supply current is identical for all members of the CAPZero family. The circuits presented in this report are therefore applicable for all family members independent of the R1+R2 external resistor values.



The current capability of the internal power MOSFETs while discharging the X capacitor do of course change throughout the family as specified in the data sheet parameter table (Drain Saturation Current specification)

Further details of CAPZero specifications and operation are available in the CAPZero data sheet and Application note AN-48.



Component Selection Table

Product ³	BV _{DSS}	Maximum Total X Capacitance	Total Series Resistance ² (R1 + R2)
CAP002DG	825 V	≤ 500 nF	1.5 MΩ
CAP012DG	1000 V		
CAP003DG	825 V	750 nF	1.02 MΩ
CAP013DG	1000 V		
CAP004DG	825 V	1 μF	780 kΩ
CAP014DG	1000 V		
CAP005DG	825 V	1.5 μF	480 kΩ
CAP015DG	1000 V		
CAP006DG	825 V	2 μF	360 kΩ
CAP016DG	1000 V		
CAP007DG	825 V	2.5 μF	300 kΩ
CAP017DG	1000 V		
CAP008DG	825 V	3.5 μF	200 kΩ
CAP018DG	1000 V		
CAP009DG	825 V	5 μF	150 kΩ
CAP019DG	1000 V		

Table 1. Component Selection Table.

Notes:

1. IEC 62301 clause 4.5 rounds standby power use below 5 mW to zero.
2. Values are nominal. RC time constant is <1 second with ±20% X capacitor and ±5% resistance from these nominal values.
3. Packages: D: SO-8.

Figure 1 – Typical CAPZero Application and Selection Table.



3 Zero Crossing (ZC) Signal Circuits

3.1 Non-Isolated Systems with Neutral as the System Ground

3.1.1 Negative Output Voltage Relative to Neutral

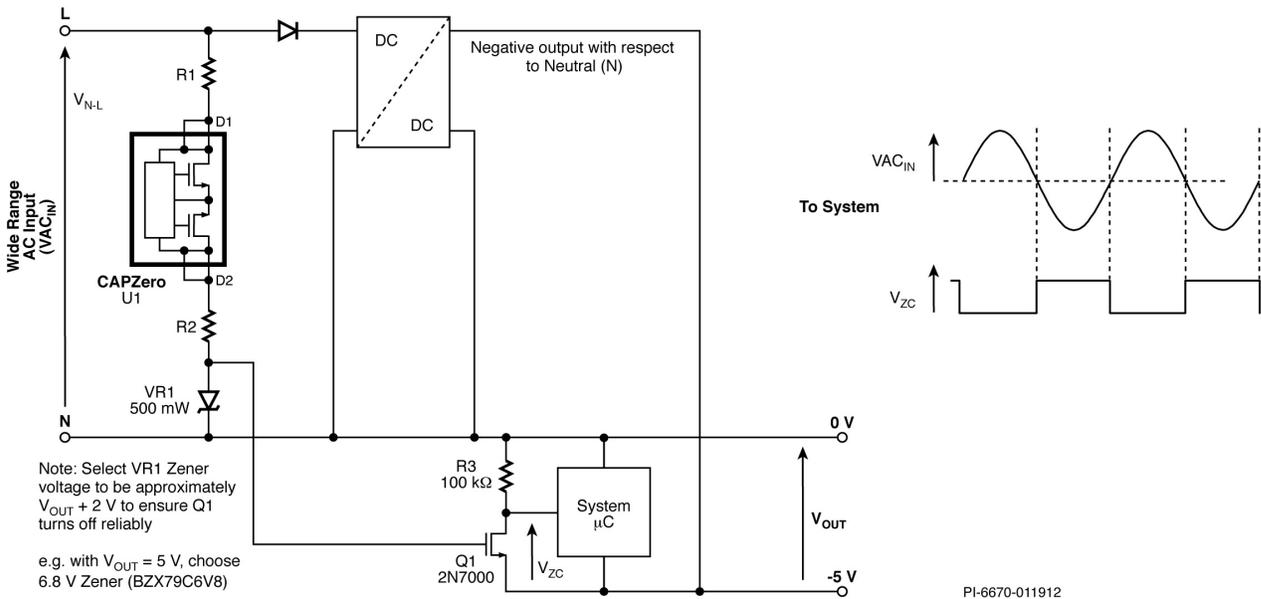


Figure 2 – Negative Output Voltage Non-isolated System Configuration.

In Figure 2 the CAPZero and R1/R2 choice are made according to the value of the system X capacitor (not shown). The V_{ZC} signal fed into the system μC is generated by switching Q1 on and off as described below.

While the AC input voltage is such that V_{N-L} is positive, the supply current ($21.7 \mu A$) of U1 flows through VR1, anode to cathode. Therefore the gate voltage (V_{GS}) of Q1 is equal to $V_{OUT} + V_{F(VR1)}$. For a nominal 5 V output, this gives a V_{GS} of 5.5 V, allowing Q1 to be a low cost logic level device. The 2N7000 device shown has a maximum gate threshold of 3 V. Applying 5.5 V will fully enhance the device, pulling down the zero cross input of the μC

During the next half-cycle (V_{N-L} is negative) the supply current of U1 flows through VR1 in the opposite direction, cathode to anode. Therefore the gate voltage (V_{GS}) of Q1 is equal to $V_{OUT} - V_{VR1}$. For a nominal 5 V output and 6.8 V Zener, the gate is therefore at -1.8 V, turning off Q1. The value of VR1 should be selected such that $V_{OUT} - V_{VR1} \leq V_{GS(TH)}$. The 2N7000 has a maximum $V_{GS(TH)}$ value of 0.8 V and a maximum V_{GS} voltage of ± 20 V.

No gate voltage clamping is required for $V_{OUT} < 18$ V. Above this, the voltage can be limited with a clamp Zener from gate to source or a resistor divider.

It is worth noting that the circuit in Figure 2 not only eliminates power consumption related to ZC signal generation but actually reduces the component count compared to normal ZC signal



circuit. Standard ZC signal circuits typically require several resistors for the high-voltage divider, plus at least one transistor and Zener to condition the divided AC signal.

Figure 3 shows measured waveforms at 115 VAC and 230 VAC with component values in Figure 2 of CAP014DG, R1 = R2 = 380 kΩ, VR1 = 6.8 V and V_{OUT} = 5 V.

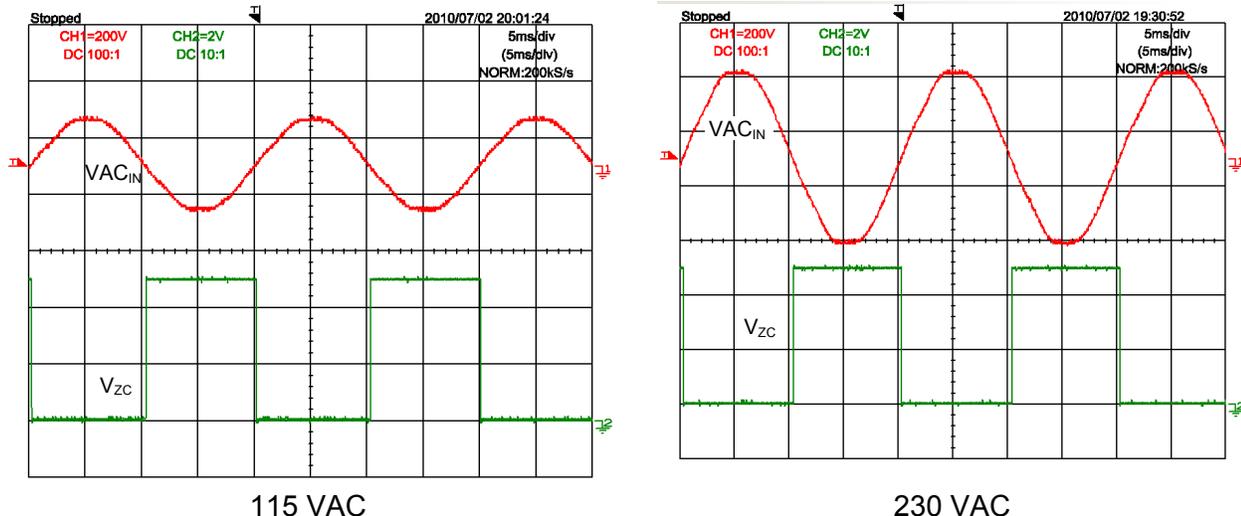


Figure 3 – V_{IN(AC)} and V_{ZC} Signals.

Figure 4 shows zoomed plots of the V_{ZC} signal transitions at the zero crossing events

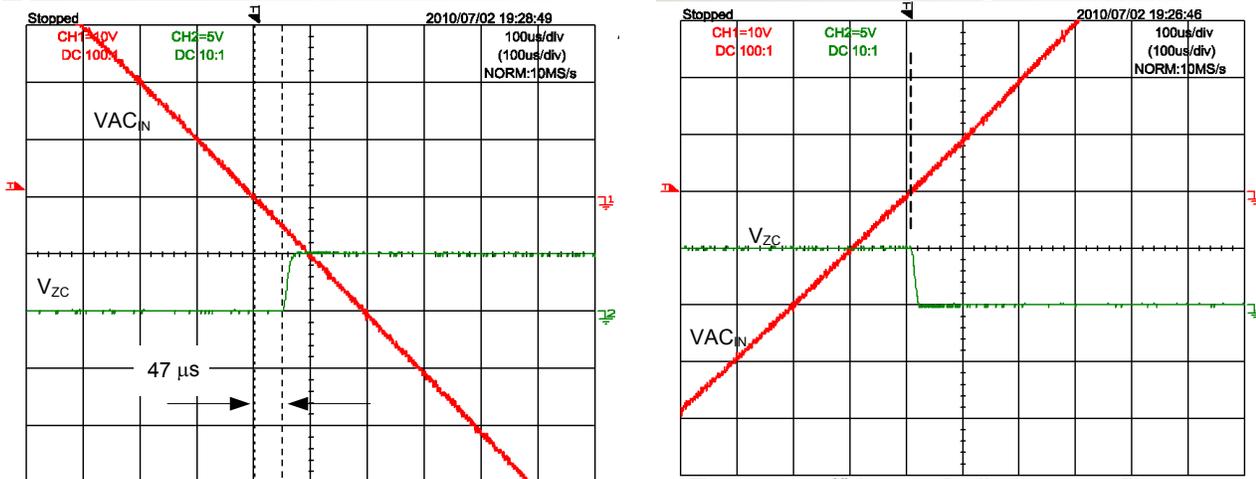


Figure 4(a) – V_{ZC} Low-High Transition.

Figure 4(b) – V_{ZC} High-Low Transition.

Figure 4 – Zoomed V_{IN(AC)} and V_{ZC} Signals at Zero Crossing Events.

Figure 4(a) shows a very small transition delay of 47 μs with a rise time in the order of 20 μs. This delay is simply a function of the time it takes to reduce the Q1 Source to Gate voltage from ~6 V (V_{OUT} plus VR1 forward voltage) to the gate threshold voltage. The rise time is largely a function of the value of R3 in Figure 2 and can be reduced with lower resistance values at the expense of some power dissipation in R3.

Figure 4(b) shows no measurable delay in the V_{ZC} high to low transition due to the very low gate threshold of Q1. Temperature effects are limited to Q1 gate threshold and VR1 variations over



temperature. One of the advantages of using a 6.8 V Zener for VR1 is the very low temperature coefficient of this Zener.

Although not shown, test results over a 0-105 °C ambient range showed that total delay in either high to low or low to high V_{ZC} transitions were below 100 μ s in all cases.

3.1.2 Positive Output Voltage Relative to Neutral

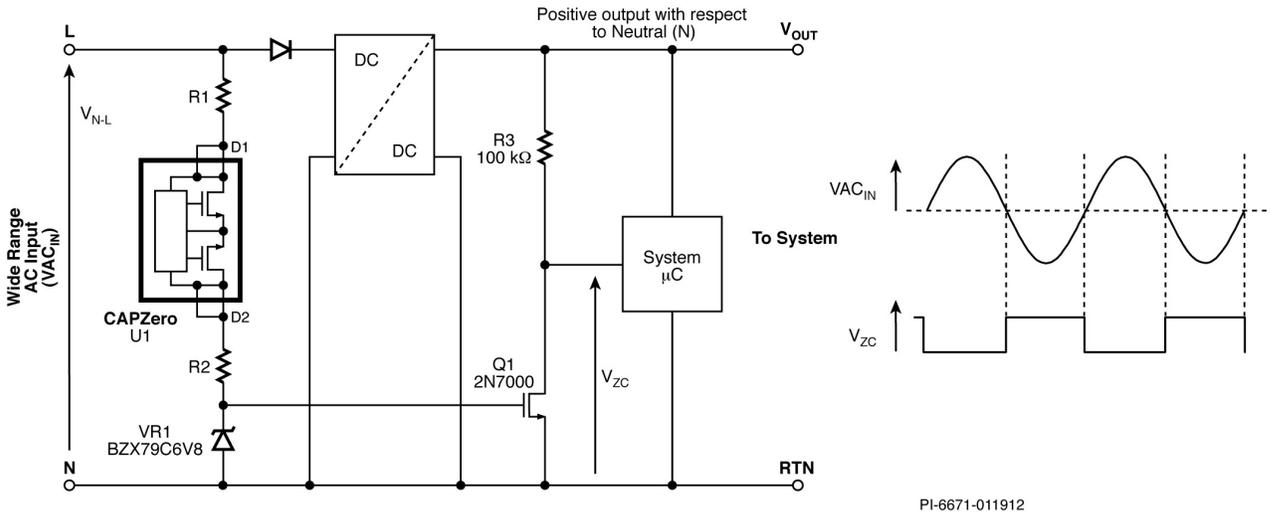


Figure 5 – Positive Output Voltage Non-isolated System Configuration.

In Figure 5 again the CAPZero and R1/R2 choice are made according to the system X capacitor being used (not shown). In common with the circuit in Figure 2, the V_{ZC} signal to the μ C is generated by switching Q1 on and off.

The function of the circuit in Figure 5 is very similar to that in Figure 2, however, the Zener diode VR1 is reversed since the Q1 turn on gate drive must now be generated as a positive signal relative to the Neutral rail. When V_{N-L} is positive, the value of $V_{GS} = VR1$, Q1 is on pulling the ZC input low. When V_{N-L} is negative, the value of $V_{GS} = V_{F(VR1)}$, i.e. the forward drop of VR1 (~0.5 V). As the threshold of Q1 is 0.8 V minimum, the value of R3 may need reducing to ensure the ZC input is pulled high even with a device with a low gate threshold.

Performance of this circuit is influenced by the same factors as the circuit in Figure 2 and as such no measured waveforms are presented.

3.2 Isolated Systems

Systems where isolation is required between the input AC line and the μ C supply voltage require opto isolated transmission of the ZC signal. The systems below describe various isolated system configurations of this type.

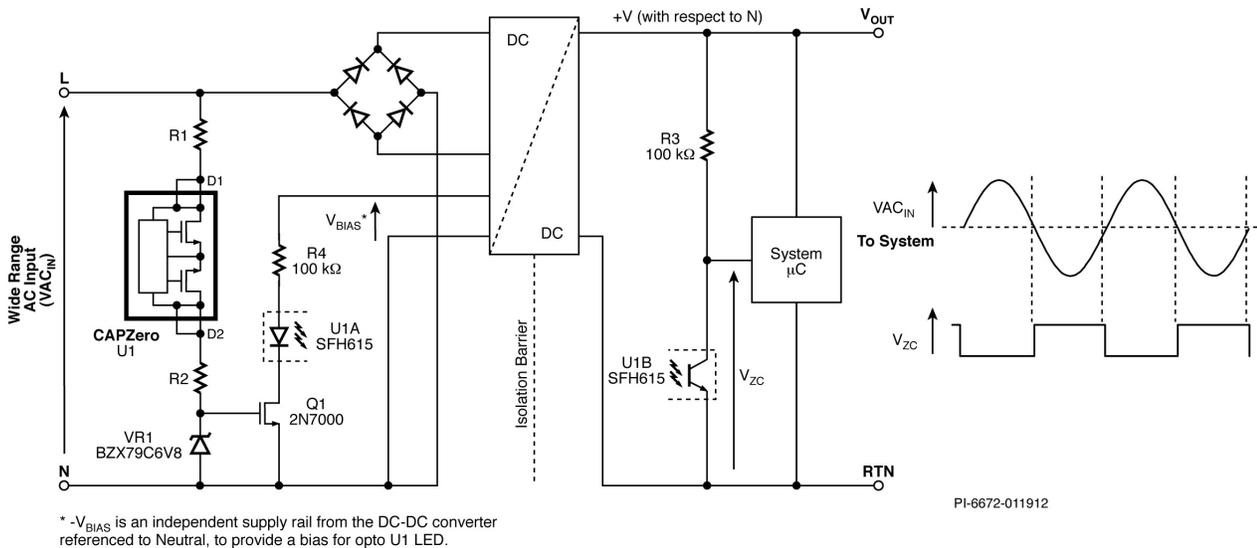
3.2.1 Isolated Systems with Full Wave Input Rectification

Figure 6 shows a system using full bridge rectification. In this case, it is necessary to provide a V_{BIAS} supply relative to input Neutral rail to provide a power source for the optocoupler U1 LED drive.



If V_{BIAS} in Figure 6 is a 10 V rail, a choice of R4 of 20 k Ω would provide a ~500 μ A LED current in U1 which is sufficient to give a reliable output with the SFH615 optocoupler shown. This current conducts for 50% of the time (only for the AC half-cycle when Q1 is on). So the average consumption of this circuit is $10\text{ V} \times 500\ \mu\text{A} \times 0.5 \times \eta$. For solutions using Power Integration devices, the value of η is >50 % even during worst case light load operation. This makes the total dissipation <5 mW.

Low cost transistor output optocoupler U1 can be replaced with a Darlington output optocoupler such as the IS127 or TLP127 to provide more margin for CTR reduction with age effecting the quality of the V_{ZC} signal. Reducing the value of R3 will provide faster V_{ZC} rising edges if required at the expense of some power consumption.



* - V_{BIAS} is an independent supply rail from the DC-DC converter referenced to Neutral, to provide a bias for opto U1 LED.

Figure 6 – Isolated System with Full Bridge Rectification.

The V_{BIAS} supply of Figure 6 must use an independent winding from the transformer of the DC-DC converter.

Figure 7 shows measured waveforms with a 9 V V_{BIAS} , 5 V μ C supply and R4 = 16 k Ω . The rise and fall times of the V_{ZC} waveform are governed by the values of R4 (that limits the optocoupler LED current) and R3 (that determines the load on the optocoupler output). Both R3 and R4 can be reduced to reduce V_{ZC} fall and rise times at the expense of power consumption both from the V_{BIAS} supply and V_{OUT} .

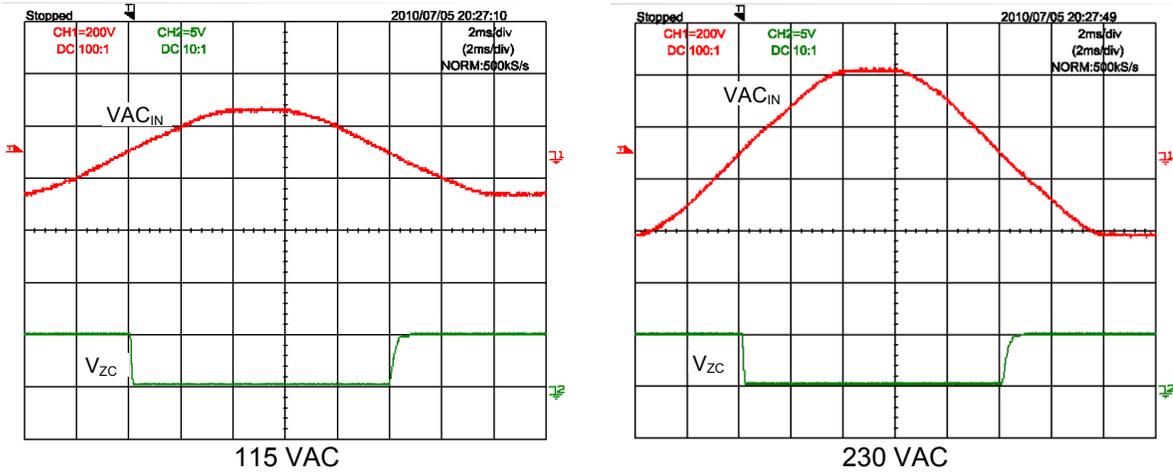


Figure 7 – V_{ZC} Signal Waveforms with System Configuration of Figure 6.

Section 3.2.2 describes an alternative configuration for isolated systems using a half wave input rectification stage.

3.2.2 Isolated Systems with Half Wave Input Rectification

Figure 8 shows an isolated system using half wave rectification. The circuit shown is a simplification of the one in Figure 6. In this case, since all primary circuitry is referenced to the input Neutral line, the existing bias supply for the primary side power supply controller can be used to generate V_{BIAS} . All other considerations are the same.

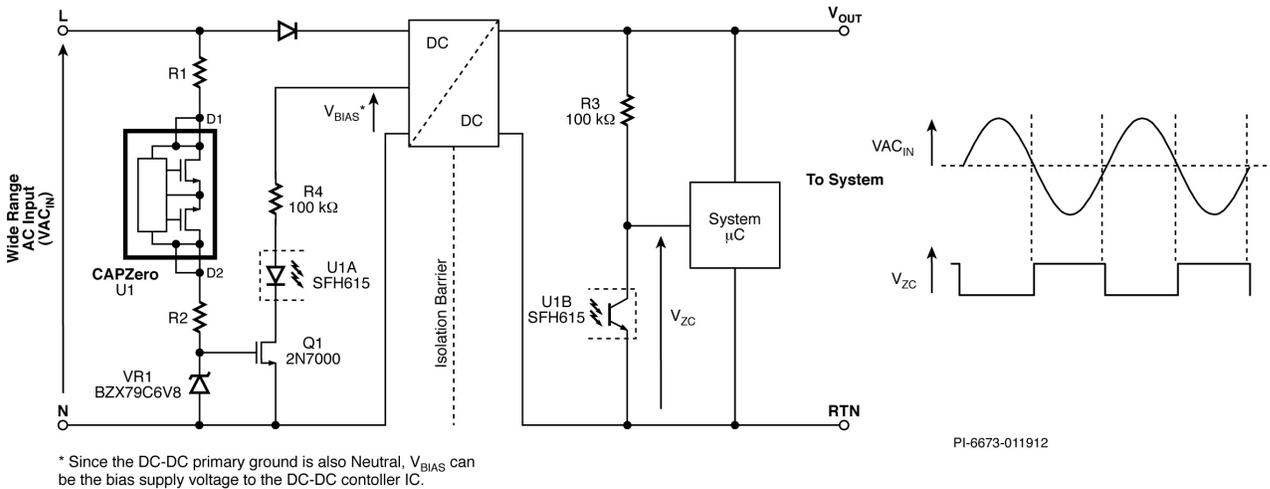


Figure 8 – Isolated System with Half Wave Input Rectification.



4 AC Fault/Loss Detection

Loss of AC input can be detected using the circuits presented in Section 3. Circuit variants can be implemented to provide more detailed information on the status and faults on the input AC as discussed below.

4.1 AC Fault Detection

AC fault detection can be necessary to recognize conditions such as temporary line drop-out or load short-circuits causing positive or negative half-cycles of the AC input voltage to be clipped.

The circuit in Figure 9 detects missing positive or negative half-cycles in a non-isolated system where the system μC is supplied with a +5 V supply relative to system Neutral. This circuit is used to describe the operation of the circuit but variants of the circuit for other types of non-isolated/isolated system configurations are then discussed.

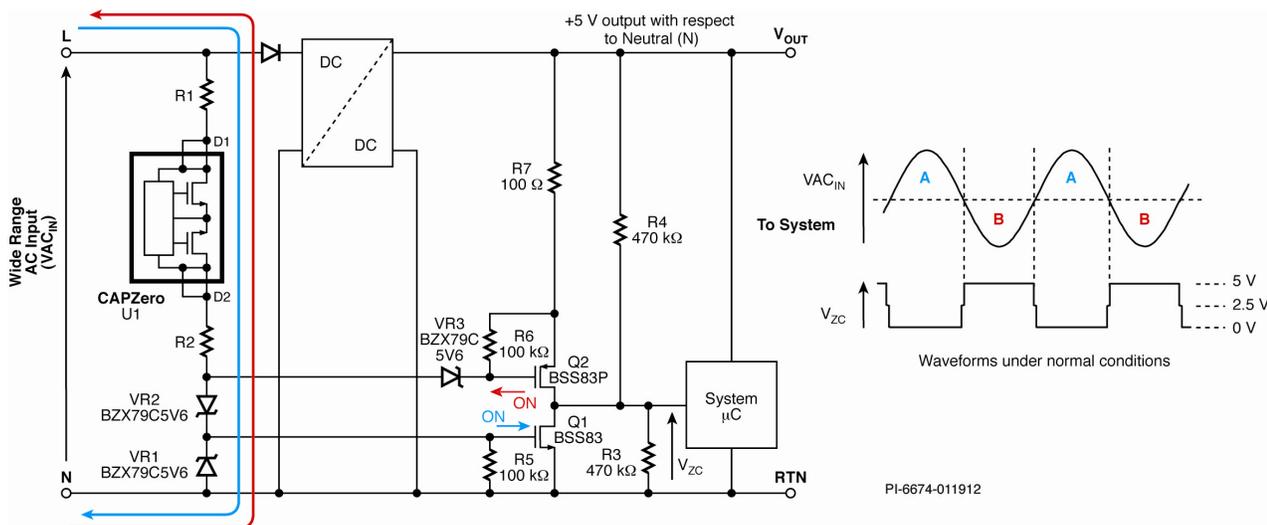


Figure 9 – AC Fault Detection in a Non-isolated positive Output Voltage System.

The V_{ZC} output waveform in Figure 9 is a pseudo square wave centered on 2.5 V. As such the absence of either positive or negative AC half-cycles can be represented to the μC without the losses normally associated with sensing the full AC line with a resistor divider.

The color coded lines and text indicate the turn on signals received by Q1 and Q2 on the relevant half-cycles of the input AC line. In phase 'A' of the AC line voltage, the gate of Q1 is taken positive relative to Neutral turning on Q1. In phase 'B' of the AC line voltage, Q1 is turned off and the anode of VR2 is $\sim(-5.6-0.7) = -6.3$ V relative to Neutral. But the gate of Q2 is 5.6 V higher due to VR3, resulting in a gate-source voltage of ~-5.7 V on Q2 which in turn switches Q2 on.



If either half-cycle of the AC line is missing, the relevant switch Q1 or Q2 does not switch and V_{ZC} assumes a 2.5 V level as defined by resistor divider R3 and R4. Resistors R5 and R6 simply ensure that the relevant MOSFET Q1 or Q2 is off if no gate signal is received. Total power consumption for the resistors R3-R7 in Figure 9 is <0.3 mW. The waveforms resulting from various AC line faults are shown in Figure 10.

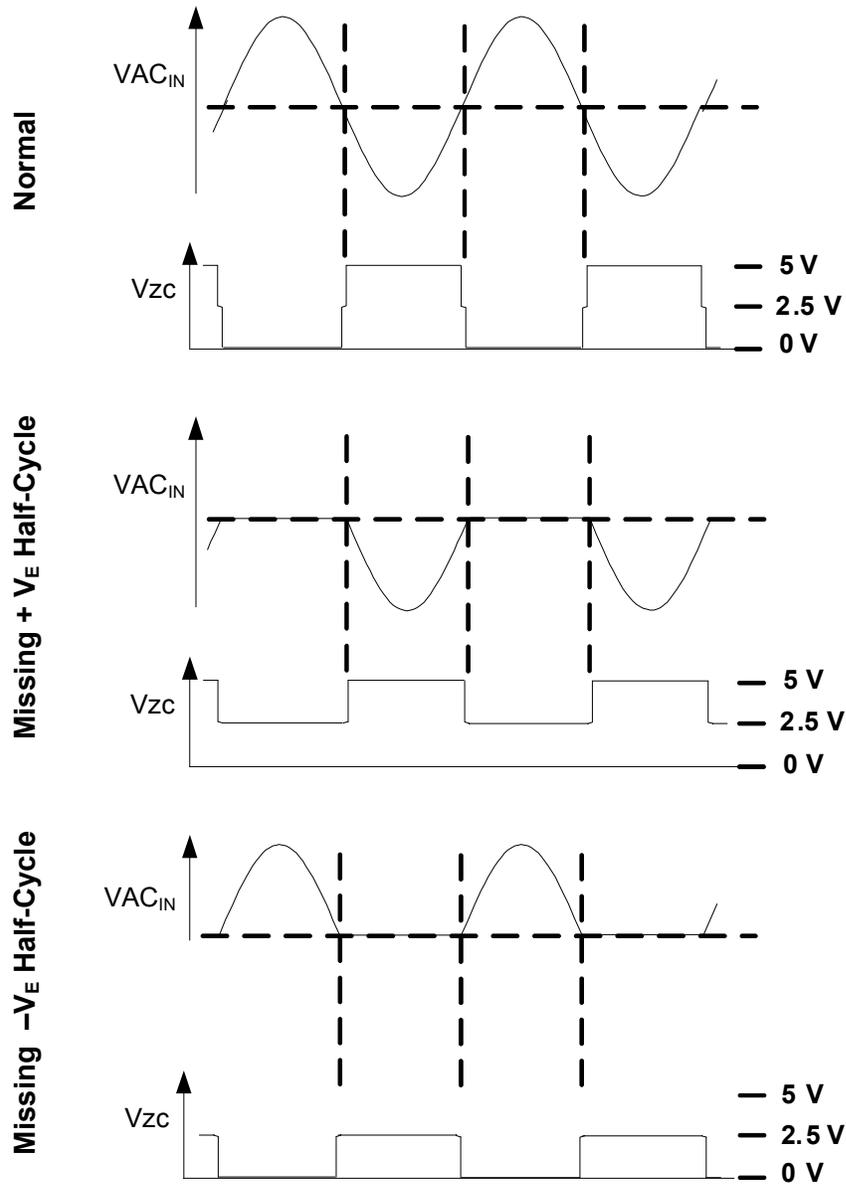


Figure 10 – Waveforms for Various AC Line Faults.

All components used in Figure 9 are low cost and selected to optimize for rugged operation over a wide temperature range. P and N-channel MOSFETs Q1 and Q2 are low cost small signal devices which can be substituted for many other low power MOSFETs such as the 2N7000 series for example as desired. It will be noted that Zener diodes VR1, VR2 and VR3 are chosen as 5.6 V devices (as opposed to the 6.8 V devices



in Section 3. This provides a slightly negative temperature coefficient in the Zener voltage to provide a similar temperature characteristic to the gate-source thresholds of Q1 and Q2 but is not critical for circuit operation. Resistor R5 limits fault current if Q1 or Q2 are short-circuited, allowing the 5 V output to the μC to be sustained for other system functions during this condition.

Figures 11 and 12 show measured results for the circuit in Figure 9. Tests were performed with $R1+R2 = 1 \text{ M}\Omega$. However tests in the range of $R1+R2 = 150 \text{ k}\Omega$ to $1.5 \text{ M}\Omega$ were carried out and the waveforms in Figure 11 and 12 are representative.

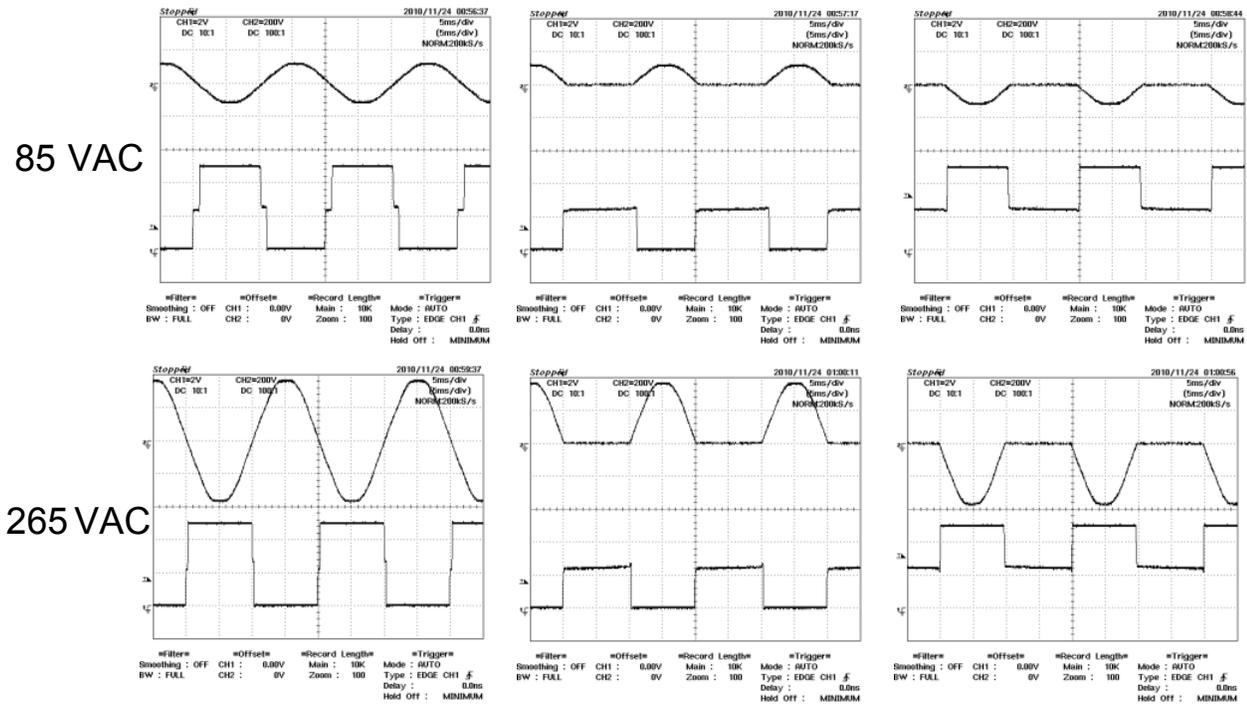


Figure 11 – Measured Waveforms at 25 °C Ambient.



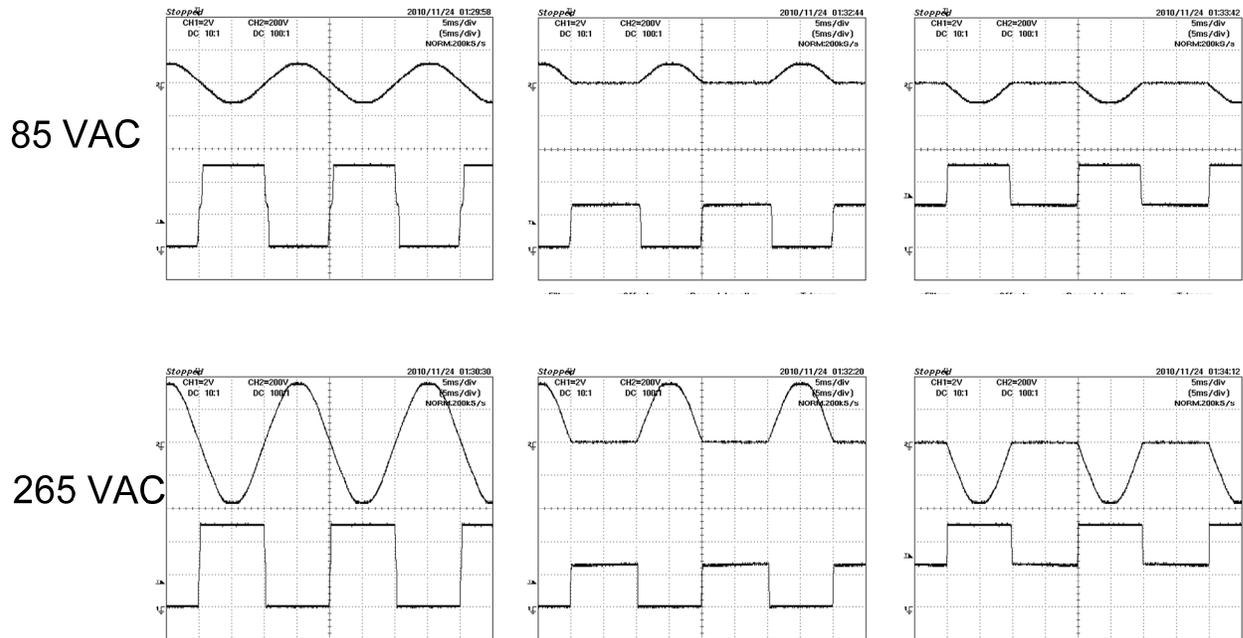


Figure 12 – Measured Waveforms at 100 °C Ambient.

Although not shown the circuit was measured with freezer spray applied as a very severe low temperature test. There were no measureable changes to the circuit performance.

Figure 13 shows an example of the AC fault detection configuration of Figure 9 but this time with an output where the μC is supplied with 5 V relative to system neutral (N).



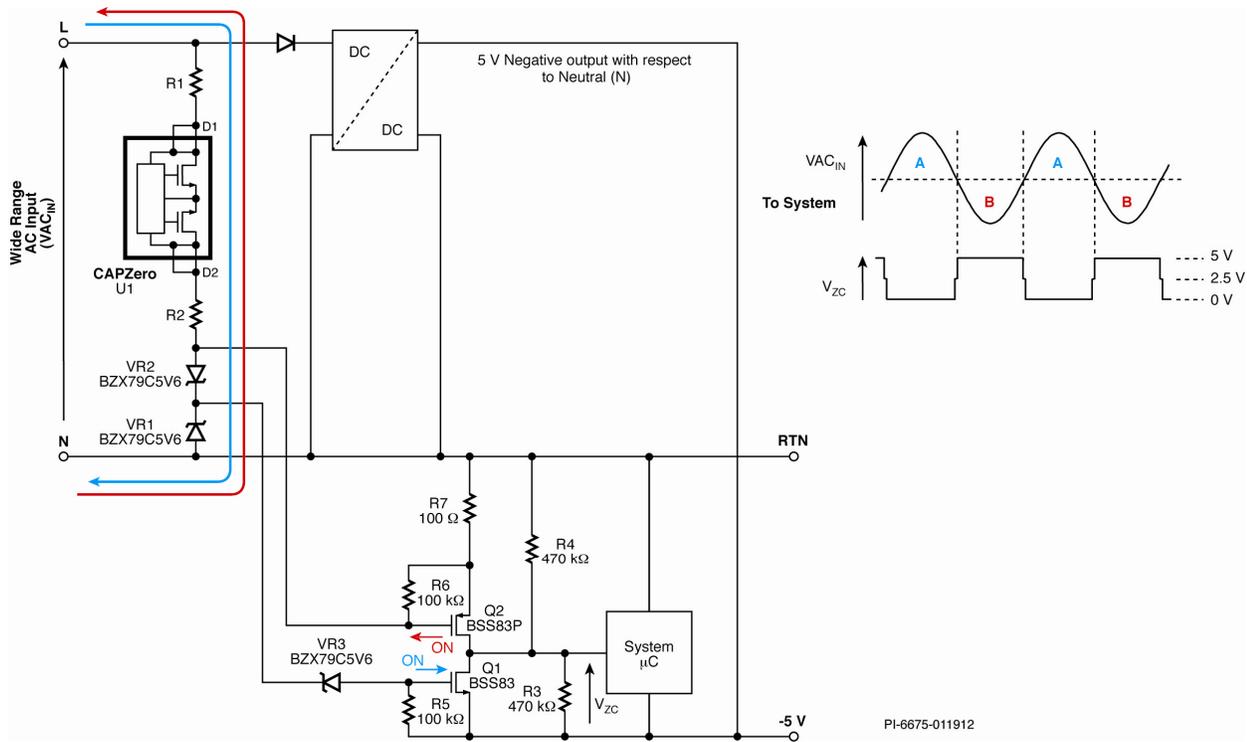


Figure 13 – AC Fault Detection in a Non-isolated negative Output Voltage System.

The circuit shares many aspects with the one in Figure 9 with the main difference that the Zener VR3 is applied to the gate of the n-channel MOSFET Q1. This ensures that under a fault where the positive ‘A’ phase of the AC input is missing, that Q1 gate is not driven and Q1 remains off as required.

The fault waveforms with respect to the μC input as identical to those shown in Figure 10.

Configurations for isolated systems are also possible requiring 2 optocouplers to differentiate between the positive or negative phased of the AC input line. These circuits would need to be designed with information on the specific system. Contact your local Power Integrations office for specific support in cases of isolated systems.

4.2 AC Loss Detection

AC loss detection is typically used to provide time for system settings and memory to be backed up before power is lost. As such any of the circuits discussed so far can be used to provide this function if the μC uses the zero crossing transitions and a timer to verify that zero crossing signals are being received regularly at a time intervals appropriate to the AC line frequency in the region of operation.



5 Further Comments and Information

- In certain cases the tests results presented above are for nominal 115 VAC and 230 VAC line voltages. However CAPZero and the ZC signal generating circuit presented operate over a very wide range from <70 VAC to >300 VAC.
- Power Integrations offer a series of high-voltage power supply controllers for use in the DC-DC blocks shown in the above descriptions. Visit www.powerint.com for further details.



6 Revision History

Date	Author	Revision	Description and Changes	Reviewed
20-Jan-12	MM	2.0	Initial Release	Apps and Mktg



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