Design Example Report

<table>
<thead>
<tr>
<th>Title</th>
<th>1.5 W Non-Isolated Flyback Power Supply with 0.00 W Power Down Mode Using LinkZero™-AX LNK584DG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>85 VAC – 265 VAC Input; 5 V, 300 mA Output</td>
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<tr>
<td>Application</td>
<td>LinkZero-AX Reference Design</td>
</tr>
<tr>
<td>Author</td>
<td>Applications Engineering Department</td>
</tr>
<tr>
<td>Document Number</td>
<td>DER-260</td>
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<tr>
<td>Date</td>
<td>October 13, 2010</td>
</tr>
<tr>
<td>Revision</td>
<td>1.3</td>
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Summary and Features

- Non-isolated design provides tight regulation.
- Low cost, low component count solution
- Power Down (PD) Mode set and reset functionality. Less than 5 mW no load consumption at 230 VAC (IEC62301 Clause 4.5 rounds standby power use below 5 mW to zero)
- Auto-restart functionality provides protection against output short circuit and open loop conditions
- Hysteretic over temperature shutdown protection
- Meets EN-550022 and CISPR-22 Class B conducted EMI with more than 10 dB margin.
- Meets IEC61000-4-5 Class 3 AC line surge specifications
PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.
1 Introduction

This report describes a universal input, 5 V, 300 mA non-isolated flyback power supply which is designed with LNK584DG device from the LinkZero-AX family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms.

Figure 1 – Prototype Top View.

Figure 2 – Prototype Bottom View.
2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

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<th>Description</th>
<th>Symbol</th>
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<td>Voltage</td>
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<td>265</td>
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<td>Output Voltage</td>
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<td>V</td>
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<td>Continuous Output Power</td>
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<td>kV</td>
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<td>Ambient Temperature</td>
<td>$T_{AMB}$</td>
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<td>50</td>
<td>°C</td>
<td>Free convection, sea level</td>
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</table>
3 Schematic

Figure 3 – Circuit Schematic.
4 Circuit Description

4.1 Input Rectification and Filtering
Diodes D1 to D4 rectify the AC input which is filtered by C1 and C2. Inductor L3, C1 and C2 form a π filter that attenuates differential mode conducted EMI. Resistor R2 provides high frequency damping. Shielding techniques (E-Shield™) were used in the construction of T1 to reduce common mode EMI displacement currents. This filter arrangement, the proprietary E-Shield techniques together with IC’s frequency jitter function provide excellent EMI performance for this solution even without a Y capacitor or a primary-side RCD clamp circuit.

4.2 LinkZero-AX Primary
The LNK584DG device (U1) integrates an oscillator, an ON/OFF controller, startup and protection circuitry and a power MOSFET all on one monolithic IC.

One side of the power transformer is connected to the positive leg of C2 and the other side is connected to the DRAIN pin of U1. At the start of a switching cycle, the controller turns the MOSFET on, and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, the controller turns the MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

4.3 Primary Clamp and Transformer Construction
A Clampless primary circuit is achieved due to the very tight tolerance current limit trimming techniques used in manufacturing the LNK584DG, together with some special transformer construction techniques that were used. Peak drain voltage is therefore limited to typically less than 550 V at 265 VAC – providing significant margin to the 700 V drain voltage (BV_DSS).

4.4 Output Rectification
Output rectification is provided by diode D6 and filtering is provided by capacitor C6. Resistor R8 and C4 provide high frequency filtering for improved EMI.

4.5 Power Down (PD) Mode – Set and Reset
LinkZero-AX goes into Power Down mode when one of the following two conditions have been met:

(i) 160 consecutive cycles have been skipped.
(ii) FB voltage exceeds 1.7 V for 160 consecutive switching cycles (approximately 2 ms).

The latter condition is the preferred way of setting the supply into “Power Down” (PD) mode. In this circuit the FB pin is pulled high through Q1 and R16. The value of the BP pin capacitor should be high enough to sustain enough current through R16 for more
than 2 ms to successfully trigger the Power Down mode. LinkZero-AX stops switching once the power down mode is triggered (PD set), and the chip cannot wake up (PD reset) until the BP pin capacitor is pulled below 1.5 V and then released to be recharged. Transistor Q2 or the mechanical switch SW1 can be used to reset the Power Down mode.

Load transients from full load to very light or no load can cause accidental triggering of the Power Down mode. To avoid this undesired effect, a preload must be used at the output of the power supply. Additionally, a capacitor (C9) in parallel to the high side feedback resistor (R9) can be used to speed up the high frequency loop response. Low value feedback resistors can act as preload too. For applications with limited load range, which guarantee that accidental power down mode will not be triggered, the preload and the capacitor in parallel to the high side feedback resistor are not necessary.

4.6 Feedback

The output voltage is sensed through resistor divider R3 and R9 and fed back to U1. Switching cycles are skipped if the FB pin disable threshold voltage (1.7 V) is exceeded. When the sensed voltage at the FB pin falls below the disable threshold, switching cycles are re-enabled. By adjusting the ratio of enabled to disable switching cycles, output regulation is maintained.

At increased loads, beyond the output power limiting point, the FB pin voltage begins to reduce as the power supply output voltage falls. As the FB pin voltage falls, the switching frequency reduces to provide some output current limiting. When the FB pin voltage drops below the auto-restart threshold (typically 0.9 V on the FB pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for 1.2 s and then turn back on for 170 ms. The auto-restart function reduces the average output current during an output short-circuit condition.
5 PCB Layout

Figure 4 – PCB Layout 2.10" (53.3 mm) x 1.81" (46.1 mm)
## 6 Bill of Materials

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<th>Qty</th>
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7 Transformer Design Spreadsheet

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<td>VO</td>
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<td>Volts</td>
<td>Output Voltage (main) measured at the end of output cable (For CV/CC designs enter typical CV tolerance limit)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>0.30</td>
<td>Amps</td>
<td>Power Supply Output Current (For CV/CC designs enter typical CC tolerance limit)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PO</td>
<td>1.50</td>
<td>Watts</td>
<td>Output Power (VO x IO + dissipation in output cable)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feedback Type</td>
<td>Direct</td>
<td>Direct</td>
<td>Choose 'Bias' for Bias winding feedback, 'Direct' for direct sensing of output and 'Opto' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clampless Design</td>
<td>Yes</td>
<td></td>
<td>Choose 'YES' from the 'Clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>0.65</td>
<td>0.65</td>
<td>Efficiency Estimate at output terminals. For CV only designs enter 0.7 if no better data available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>0.5</td>
<td></td>
<td>Loss Allocation Factor (Secondary side losses / Total losses)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tC</td>
<td>2.90</td>
<td>mSeconds</td>
<td>Bridge Rectifier Conduction Time Estimate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>6.60</td>
<td>uFara</td>
<td>Input Capacitance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENTER LinkZero-AX VARIABLES</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LinkZero-AX</td>
<td>Auto</td>
<td>LNK584</td>
<td>LinkZero-AX device</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIMITMIN</td>
<td>0.126</td>
<td>Amps</td>
<td>Minimum Current Limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIMITMAX</td>
<td>0.146</td>
<td>Amps</td>
<td>Maximum Current Limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>fSmin</td>
<td>93000</td>
<td>Hertz</td>
<td>Minimum Device Switching Frequency. May be lower than 93 kHz for high line (230 VAC) designs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I^2fMIN</td>
<td>1664.64</td>
<td>A^2Hz</td>
<td>I^2f Minimum value (product of current limit squared and frequency is trimmed for tighter tolerance)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I^2fTYP</td>
<td>1849.6</td>
<td>A^2Hz</td>
<td>I^2f typical value (product of current limit squared and frequency is trimmed for tighter tolerance)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOR</td>
<td>61.00</td>
<td>Volts</td>
<td>Reflected Output Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDS</td>
<td>10</td>
<td>Volts</td>
<td>LinkZero-AX on-state Drain to Source Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>0.5</td>
<td>Volts</td>
<td>Output Winding Diode Forward Voltage Drop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>KP</td>
<td>1.58</td>
<td></td>
<td>Ripple to Peak Current Ratio (0.9&lt;\text{KRP}&lt;1.0 ; 1.0&lt;\text{KDP}&lt;6.0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core Type</td>
<td>EE16</td>
<td>EE16</td>
<td>User-Selected transformer core</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core</td>
<td>EE16</td>
<td></td>
<td>P/N: PC40EE16-Z</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bobbin</td>
<td>EE16_BOBBIN</td>
<td></td>
<td>P/N: EE16_BOBBIN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AE</td>
<td>0.192</td>
<td>cm^2</td>
<td>Core Effective Cross Sectional Area</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LE</td>
<td>3.5</td>
<td>cm</td>
<td>Core Effective Path Length</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AL</td>
<td>1140</td>
<td>nH/T^2</td>
<td>Ungapped Core Effective Inductance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>8.6</td>
<td>mm</td>
<td>Bobbin Physical Winding Width</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>0</td>
<td>mm</td>
<td>Safety Margin Width (Half the Primary to Secondary Creepage Distance)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>2</td>
<td></td>
<td>Number of primary layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NS</td>
<td>10.00</td>
<td>10</td>
<td>Number of Secondary Turns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NB</td>
<td>28</td>
<td></td>
<td>Number of Bias winding turns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VB</td>
<td>15.13</td>
<td>Volts</td>
<td>Bias Winding Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>1.00</td>
<td>kΩ</td>
<td>Calculated standard value (1%) of Upper Resistor in the resistor divider component between bias winding and FB pin</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### DC INPUT VOLTAGE PARAMETERS
- **VMIN**: 97 Volts (Minimum DC Input Voltage)
- **VMAX**: 375 Volts (Maximum DC Input Voltage)

### CURRENT WAVEFORM SHAPE PARAMETERS
- **DMAX**: 0.33 (Maximum Duty Cycle)
- **IAVG**: 0.03 Amps (Average Primary Current)
- **IP**: 0.13 Amps (Minimum Peak Primary Current)
- **IR**: 0.13 Amps (Primary Ripple Current)
- **IRMS**: 0.04 Amps (Primary RMS Current)

### TRANSFORMER PRIMARY DESIGN PARAMETERS
- **LP**: 2287 uHenries (Typical Primary Inductance, +/- 10%)
- **LP TOLERANCE**: 10 % (Primary inductance tolerance)
- **NP**: 111 (Primary Winding Number of Turns)
- **ALG**: 186 nH/T² (Gapped Core Effective Inductance)
- **BM**: 1568 Gauss (Maximum Operating Flux Density, BM<2000 is recommended)
- **BAC**: 784 Gauss (AC Flux Density for Core Loss Curves (0.5 X Peak to Peak))
- **ur**: 1654 (Relative Permeability of Ungapped Core)
- **LG**: 0.12 mm (Gap Length (Lg > 0.08 mm))
- **BWE**: 17.2 mm (Effective Bobbin Width)
- **OD**: 0.16 mm (Maximum Primary Wire Diameter including insulation)
- **INS**: 0.04 mm (Estimated Total Insulation Thickness (= 2 * film thickness))
- **DIA**: 0.12 mm (Bare conductor diameter)
- **AWG**: 37 AWG (Primary Wire Gauge (Rounded to next smaller standard AWG value))
- **CM**: 20 Cmils (Bare conductor effective area in circular mils)
- **CMA**: 452 Cmils/Amp (Primary Winding Current Capacity (150 < CMA < 500))

### TRANSFORMER SECONDARY DESIGN PARAMETERS
- **ISP**: 1.40 Amps (Peak Secondary Current)
- **ISRMS**: 0.59 Amps (Secondary RMS Current)
- **IRIPPLE**: 0.51 Amps (Output Capacitor RMS Ripple Current)
- **CMS**: 118 Cmils (Secondary Bare Conductor minimum circular mils)
- **AWGS**: 29 AWG (Secondary Wire Gauge ( Rounded up to next larger standard AWG value))
- **DIAS**: 0.29 mm (Secondary Minimum Bare Conductor Diameter)
- **ODS**: 0.86 mm (Secondary Maximum Outside Diameter for Triple Insulated Wire)
- **INSS**: 0.29 mm (Maximum Secondary Insulation Wall Thickness)

### VOLTAGE STRESS PARAMETERS
- **VDRAIN**: - Volts (Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.)
- **PIVS**: 39 Volts (Output Rectifier Maximum Peak Inverse Voltage)
8 Transformer Specification

8.1 Electrical Diagram

![Transformer Electrical Diagram]

**Figure 5** – Transformer Electrical Diagram.

8.2 Electrical Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Strength</td>
<td>1 second, 60 Hz, from pins 1-5 to pins 6-10</td>
<td>3000 VAC</td>
</tr>
<tr>
<td>Primary Inductance</td>
<td>Pins 3-1, all other windings open, measured at 100 kHz, 0.4 VRMS</td>
<td>2.287 mH, ±10%</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>Pins 3-1, all other windings open</td>
<td>300 kHz (Min.)</td>
</tr>
<tr>
<td>Primary Leakage Inductance</td>
<td>Pins 1-3, with pins 10-8 shorted, measured at 100 kHz, 0.4 VRMS</td>
<td>50 μH (Max.)</td>
</tr>
</tbody>
</table>

8.3 Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>Core: PC44 EE16, TDK or equivalent Gapped for ALG of 186 nH/T^2</td>
</tr>
<tr>
<td>[5]</td>
<td>Tape: 3M 1298 Polyester Film, 2.0 mils thick, 9.8 mm wide</td>
</tr>
</tbody>
</table>
8.4 Transformer Build Diagram

![Transformer Build Diagram](image)

8.5 Transformer Construction

<table>
<thead>
<tr>
<th>Bobbin Preparation</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>WD #1 Feedback</td>
<td>Start on pin 3, wind 18 bifilar turns of item [3] from left to right. Wind with tight tension across entire bobbin evenly. Finish on pin 2.</td>
</tr>
<tr>
<td>Insulation</td>
<td>1 layer of tape [5] for insulation</td>
</tr>
<tr>
<td>WD #2 Primary</td>
<td>Start on pin 1, wind 37 turns of item [3] from left to right. After finishing the first layer, placing one layer of tape [5]. Continue to wind the second layer the wire from right to left with another 37 turns. After finishing the second layer, placing one layer of tape [5]. Continue to wind the wire from left to right with another 37 turns. Finish on pin 3.</td>
</tr>
<tr>
<td>Insulation</td>
<td>1 layer of tape [5] for insulation</td>
</tr>
<tr>
<td>WD #3 Secondary</td>
<td>Start at pin 8, wind 10 bifilar turns of item [4] from left to right. Wind uniformly. After finishing the 10th turn, bring the wire back and finish it on pin 10.</td>
</tr>
<tr>
<td>Insulation</td>
<td>3 layers of tape [5] for insulation</td>
</tr>
<tr>
<td>Grind core</td>
<td>Grind the core to get 2.265 mH. Secure the core with tape. Vanish.</td>
</tr>
<tr>
<td>Finish</td>
<td>Secure the core with tape. Vanish.</td>
</tr>
</tbody>
</table>
9  Performance Data
All measurements performed at room temperature and 50 Hz input frequency, except where otherwise stated. For all tests, the full load is 300 mA.

9.1  Active Mode Efficiency

![Graph showing active mode efficiency vs. load and input voltage](image)

**Figure 7** - Efficiency vs. Input Voltage, Room Temperature, 50 Hz.

<table>
<thead>
<tr>
<th>Percent of Full Load</th>
<th>115 VAC</th>
<th>230 VAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>60.7</td>
<td>55.0</td>
</tr>
<tr>
<td>50</td>
<td>67.1</td>
<td>63.3</td>
</tr>
<tr>
<td>75</td>
<td>69.5</td>
<td>66.3</td>
</tr>
<tr>
<td>100</td>
<td>70.0</td>
<td>67.7</td>
</tr>
<tr>
<td>Average</td>
<td>66.8</td>
<td>63.1</td>
</tr>
</tbody>
</table>
9.2 No-load Input Power (Not in Power Down Mode)

Figure 8 – No-load Input Power vs. Input Line Voltage, 25°C, 50 Hz.
9.3 No-load Input Power in Power Down Mode

The chart below shows the no load input power when in power down mode. In this mode, the input power is typically less than 5 mW at 230 VAC. The input power must be tested after 30 minutes to allow for the leakage currents of the bulk capacitors to stabilize. Power readings taken before this period will be higher. Also all measurements must be made without any multi meter or probes attached to the board as these tend to load the input.

![Graph showing no-load input power vs. input voltage](image)

**Figure 9** – No-load Input Power in PD mode vs. Input Line Voltage, 25 °C, 50 Hz. 30 Minute Dwell Time at 230 VAC Prior to Taking Measurements.
9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 0.5 W and 1.0 W.

![Graph](image)

**Figure 10** – Available Output Power for 0.5 W and 1 W Input Power.
9.5 Line Regulation

![Graph showing line regulation](image)

**Figure 11** – Full Load Regulation at Room Ambient.
9.6 Load Regulation

Figure 12 – Load Regulation at Room Ambient.
10 Thermal Performance

Temperature measurements of key components were taken using T-type (Copper-Constantan) thermocouples. The thermocouples were soldered directly to a Source pin of the LNK584DG device and to the cathode of the output rectifier. The thermocouples were glued to the external core and to winding surfaces of the transformer.

The unit was sealed inside a large box to eliminate any air currents. The box was placed inside a thermal chamber. The ambient temperature within the large box was raised to 50 °C. The unit was then operated at full load and the temperature measurements were taken after they stabilized for 1 hour at 50 °C.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>85 VAC</th>
<th>265 VAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient inside the box</td>
<td>51.0</td>
<td>51.0</td>
</tr>
<tr>
<td>LNK584DG (U1)</td>
<td>64</td>
<td>68</td>
</tr>
<tr>
<td>Output diode</td>
<td>71</td>
<td>73</td>
</tr>
<tr>
<td>Transformer</td>
<td>60</td>
<td>61</td>
</tr>
</tbody>
</table>

These results show that the IC has an acceptable rise in temperature.
11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

**Figure 13** – 85 VAC, Full Load.
Upper: $V_{\text{DRAIN}}$, 100 V / div.
Lower: $I_{\text{DRAIN}}$, 0.1 A, 10 μs / div.

**Figure 14** – 265 VAC, Full Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.1 A, 10 μs / div.
11.2 Output Voltage Start-up Profile with Input Voltage

Figure 15 – Start-up Profile, 85 VAC, Full load, 1 V / div., 2 ms / div.

Figure 16 – Start-up Profile, 115 VAC, Full load, 1 V / div., 2 ms / div.

Figure 17 – Start-up Profile, 230 VAC, Full load, 1 V / div., 2 ms / div.

Figure 18 – Start-up Profile, 265 VAC, Full load, 1 V / div., 2 ms / div.
11.3 Power Down Mode Reset via Q2

When U1 is reset from the power down mode, notice how the output starts increasing after the BP pin voltage reaches 5.8 V.

**Figure 19** – Start-up Profile, 85 VAC, Full Load,
Upper: $V_O$, 1 V / div., 2 ms / div.
Lower: $V_{BP}$, 5 V / div.

**Figure 20** – Start-up Profile, 115 VAC, Full Load,
Upper: $V_O$, 1 V / div., 2 ms / div.
Lower: $V_{BP}$, 5 V / div.

**Figure 21** – Start-up Profile, 230 VAC, Full Load,
Upper: $V_O$, 1 V / div., 2 ms / div.
Lower: $V_{BP}$, 5 V / div.

**Figure 22** – Start-up Profile, 265 VAC, Full Load,
Upper: $V_O$, 1 V / div., 2 ms / div.
Lower: $V_{BP}$, 5 V / div.
11.4 Power Down Mode Set via Switch Q1

**Figure 23** – Power Down Latch Off, 85 VAC, Full Load, 1 V / div., 50 ms / div.

**Figure 24** – Power Down Latch Off, 115 VAC, Full Load, 1 V / div., 50 ms / div.

**Figure 25** – Power Down Latch Off, 230 VAC, Full Load, 1 V / div., 50 ms / div.

**Figure 26** – Power Down Latch Off, 265 VAC, Full Load, 1 V / div., 50 ms / div.
11.5 Drain Voltage and Current Start-up Profile

**Figure 27** – 85 VAC Input and Maximum Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.1 A, 1 ms / div.

**Figure 28** – 265 VAC Input and Maximum Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.1 A, 1 ms / div.
11.6 Load Transient Response

11.6.1 ~ 0% to 100% Load Step

Figure 29 – Transient Response, 85 VAC, 
4 mA – 300 mA – 4 mA, 
Upper: $V_O$, 20 mV / div., 100 ms / div. 
Lower: $I_O$, 0.2 A / div.

Figure 30 – Transient Response, 115 VAC 
4 mA – 300 mA – 4 mA, 
Upper: $V_O$, 20 mV / div., 100 ms / div. 
Lower: $I_O$, 0.2 A / div.

Figure 31 – Transient Response, 230 VAC, 
4 mA – 300 mA – 4 mA, 
Upper: $V_O$, 20 mV / div., 100 ms / div. 
Lower: $I_O$, 0.2 A / div.

Figure 32 – Transient Response, 265 VAC, 
4 mA – 300 mA – 4 mA, 
Upper: $V_O$, 20 mV / div., 100 ms / div. 
Lower: $I_O$, 0.2 A / div.
11.6.2 50% to 100% Load Step

**Figure 33** – Transient Response, 85 VAC, 150 mA – 300 mA – 150 mA, Upper: $V_o$, 20 mV / div., 100 ms / div. Lower: $I_o$, 0.2 A / div.

**Figure 34** – Transient Response, 115 VAC, 150 mA – 300 mA – 150 mA, Upper: $V_o$, 20 mV / div., 100 ms / div. Lower: $I_o$, 0.2 A / div.

**Figure 35** – Transient Response, 230 VAC, 150 mA – 300 mA – 150 mA, Upper: $V_o$, 20 mV / div., 100 ms / div. Lower: $I_o$, 0.2 A / div.

**Figure 36** – Transient Response, 265 VAC, 150 mA – 300 mA – 150 mA, Upper: $V_o$, 20 mV / div., 100 ms / div. Lower: $I_o$, 0.2 A / div.
11.6.3 100% to 0% (No-Load) Load Step
This following transient load tests verify that under extreme conditions of transient loads, power down mode is not triggered.

**Figure 37** – Transient Response, 85 VAC,
300 mA – 0 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

**Figure 38** – Transient Response, 115 VAC,
300 mA – 0 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

**Figure 39** – Transient Response, 230 VAC,
300 mA – 0 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

**Figure 40** – Transient Response, 265 VAC,
300 mA – 0 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.
11.6.4 0% to 100% Load Step

Figure 41 – Transient Response, 85 VAC,
0 mA – 300 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

Figure 42 – Transient Response, 115 VAC,
0 mA – 300 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

Figure 43 – Transient Response, 230 VAC,
0 mA – 300 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.

Figure 44 – Transient Response, 265 VAC,
0 mA – 300 mA
Upper: $V_O$, 20 mV / div., 50 ms / div.
Lower: $I_O$, 0.2 A / div.
11.7 Output Ripple Measurements

11.7.1 Ripple Measurement Technique
For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 46 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)
11.7.2 Measurement Results at 25°C Ambient Temperature

**Figure 47** – Output Ripple, 85 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

**Figure 48** – Output Ripple, 115 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

**Figure 49** – Output Ripple, 230 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

**Figure 50** – Output Ripple, 265 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.
11.8 **Output Short-Circuit at Room Ambient**

In the event of a short circuit on the output, the LNK584DG enters auto-restart mode. In this protection model, switching is disabled. The auto-restart alternately enables and disables the switching of the power MOSFET at a duty cycle of typically 12% until the fault condition is removed.

11.8.1 Auto-Restart On/Off Time Test

![Auto-Restart On/Off Time Test](image)

**Figure 51** – 85 VAC Input, Short-Circuit.
Upper: $V_{\text{DRAIN}}$, 100 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A, 500 ms / div.
Auto-restart On Time, 313 ms. Auto-restart Off Time, 1.9 s.

**Figure 52** – 265 VAC Input and Maximum Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A, 20 μs / div.
Auto-restart On Time, 395 ms. Auto-restart Off Time, 2.4 s
11.8.2 Drain Voltage and Current Under Output Short-Circuit

The waveforms show that there is no saturation of the transformer under output short circuit and the voltage stress is also below the 700 V $BV_{DSS}$ rating of the LNK584DG.

**Figure 53** – 85 VAC Input and Maximum Load.
Upper: $V_{DRAIN}$, 100 V / div.
Lower: $I_{DRAIN}$, 0.05 A, 5 ms / div.

**Figure 54** – 85 VAC Input and Maximum Load.
Upper: $V_{DRAIN}$, 100 V / div.
Lower: $I_{DRAIN}$, 0.05 A, 20 $\mu$s / div.

**Figure 55** – 265 VAC Input and Maximum Load.
Upper: $V_{DRAIN}$, 200 V / div.
Lower: $I_{DRAIN}$, 0.05 A, 5 ms / div.

**Figure 56** – 265 VAC Input and Maximum Load.
Upper: $V_{DRAIN}$, 200 V / div.
Lower: $I_{DRAIN}$, 0.05 A, 1 $\mu$s / div.
12 Line Surge

Input line 1.2/50 μs common-mode and differential mode surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event. Test conditions and results are shown below.

<table>
<thead>
<tr>
<th>Surge Level (V)</th>
<th>Input Voltage (VAC)</th>
<th>Injection Location</th>
<th>Line Impedance (Ω)</th>
<th>Injection Phase (°)</th>
<th>Number of Surges</th>
<th>Test Result (Pass/Fail)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+1000</td>
<td>230</td>
<td>L to N</td>
<td>2</td>
<td>90</td>
<td>10</td>
<td>Pass</td>
</tr>
<tr>
<td>-1000</td>
<td>230</td>
<td>L to N</td>
<td>2</td>
<td>270</td>
<td>10</td>
<td>Pass</td>
</tr>
<tr>
<td>+2000</td>
<td>230</td>
<td>L/N to GND</td>
<td>12</td>
<td>90</td>
<td>10</td>
<td>Pass</td>
</tr>
<tr>
<td>-2000</td>
<td>230</td>
<td>L/N to GND</td>
<td>12</td>
<td>270</td>
<td>10</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Units passed under all test conditions.
13 EMI Tests at Full Load

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load. Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

13.1 EMI Results

Figure 57 – Conducted EMI at 115 VAC 60 Hz, 0.3 A Load, Secondary Ground Connected to Artificial Hand.
Figure 58 – Conducted EMI at 230 VAC 60 Hz, 0.3 A Load, Secondary Ground Connected to Artificial Hand.

Figure 59 – Conducted EMI at 115 VAC 60 Hz, 0.3 A Load, Secondary Ground Floating.
Figure 60 – Conducted EMI at 230 VAC 60 Hz, 0.3 A Load, Secondary Ground Floating
## 14 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Author</th>
<th>Revision</th>
<th>Description &amp; changes</th>
<th>Reviewed</th>
</tr>
</thead>
<tbody>
<tr>
<td>13-Oct-10</td>
<td>PL</td>
<td>1.3</td>
<td>Initial Release</td>
<td>Apps &amp; Mktg</td>
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</table>
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